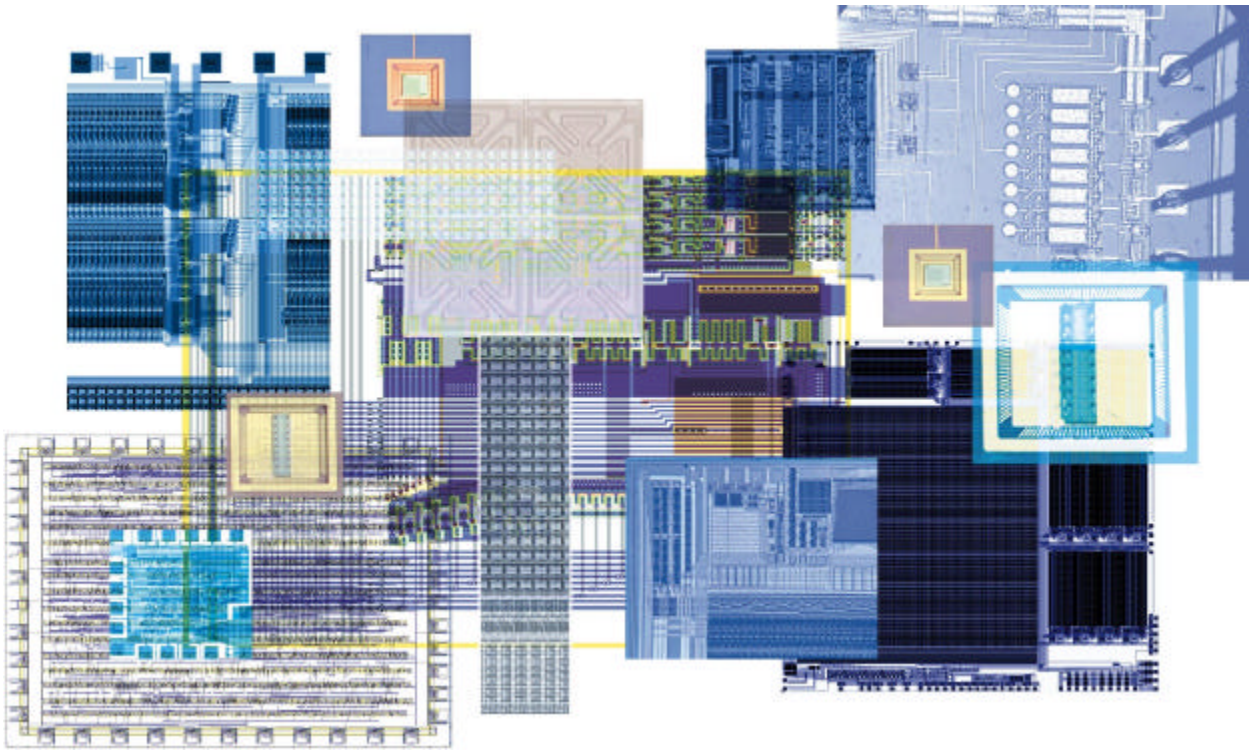
Tanner Consulting & Engineering Services

Presenting

MAMIS035DL Digital Low Power Standard Cell Library For Mosis AMI 0.5µ Sub-micron Process

Revision A



mAMIs 0.5µ

TANNER CES GENERAL TERMS & CONDITIONS

Liability

All designs will be implemented under the Client's front-end specification. Our contracted engineering services are accomplished for the Client on a best effort basis. Quality assurance is achieved by arriving at a common understanding of the nature of the Project among the engineers and managers at the Client operation and at Tanner CES. Tanner Research is not liable for the functionality, quality, or performance of the Client's future Projects using components produced as part of the contracted work. Tanner Research is not liable if the Client chooses to use our recommended design or application methodologies. If prototype chips are delivered, the process vendors do not generally guarantee yield, quality, or performance of their products. Neither does Tanner Research extend any warrantee to the contracted design and its fabricated results.

Non-Disclosure Agreement

Non-disclosure agreements (NDAs) serve the following purposes.

- Signed between the Client and Tanner Research, the NDA protects Client's original concept, status, and intentions in current and future product development and manufacturing.
- Signed between the Client and Tanner Research, the NDA protects Tanner Research' specific technologies, IC libraries, building blocks and methodologies that are developed prior to the Client Project, or developed specifically for the Client application.
- Specific non-disclosure or non-distribution conditions may be added to the Statement of Work for individual Client Projects. These conditions do not replace or supercede any previously signed NDA; rather they serve as additional constraints to the NDA.
- During or at the end of the Client Project, if we communicate with a process vendor or receive fabricated parts from a process vendor which will be forwarded to the Client, we assume that the Client is also a current customer of the vendor. We may request Client to provide a proof of its NDA with the vendor before any such communication or transaction.

Ownership of Work Results

The Client owns the delivered version and the fabricated version of the work results from a contracted Client Project. These results are subject to the following re-distribution conditions:

- The Client agrees to use the work results only in its own Projects or products, as developed by the Client and on the Client's own site.
- The Client will not distribute copies of the delivered data files and documents (such as design, libraries, process technology setups, design flows and methodologies, software utilities, etc.) to any third parties or to any other Client site, with the following two exceptions:

  Exception 1: If applicable, results can be delivered to the Government Agency sponsoring the Client Project, if such delivery is negotiated as part of the Client Project. During contract negotiations, the Client shall inform Tanner Research about such a delivery and receive advance agreement from us for the contents to be disclosed.

  Exception 2: If applicable, results can be incorporated into published academic research or presented for academic purposes. During contract negotiation, the Client shall inform Tanner Research about such a presentation and receive advanced agreement from us for the contents to be disclosed.

  Any other exceptions shall be specified in a written document signed by both the Client and Tanner Research.

Tanner Research does not own the original design and application concepts from the Client. We agree not to disclose the Client's proprietary design and applications information. However, we shall distinguish the following items that remain the property of Tanner Research:

- The methodology used through the development of the Client Project, or that we planned for Client to apply the Project's results, are usually either common knowledge in the industry or specific methods invented by Tanner Research. Using or adopting these methodologies in the Client Project does not institute the Client's ownership to these methodologies.
- Client does not own Tanner Research's general-purpose building elements (such as cell libraries, building blocks, IO pad cells, etc.) that we utilize in a contracted Project. These building elements are Tanner Research's current design resources that are widely used internally and/or distributed as commercial products. Using these building elements does not institute the Client's ownership of them.

Protect Tanner Research's Engineering Resources

Through the entire Client Project cycle, starting from bid and proposal to the end of the Project, the Client will contact various engineering resources within Tanner Research. These resources may include Tanner Research's employees and its associates (subcontracting firms or individuals). The Client agrees not to recruit or hire any of these individuals or contract with any firms during the three years following Project completion.

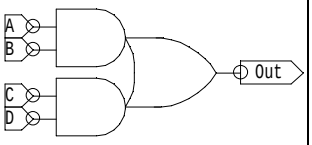
☐☑

Table of Contents

Description: 2 X 2 Input AND-OR Gate

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	AO22
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	AO22
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A*B	C*D	Out
0	0	0
1	X	1
X	1	1

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953
D	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	57 λ	3021 λ^2	2.5	1X

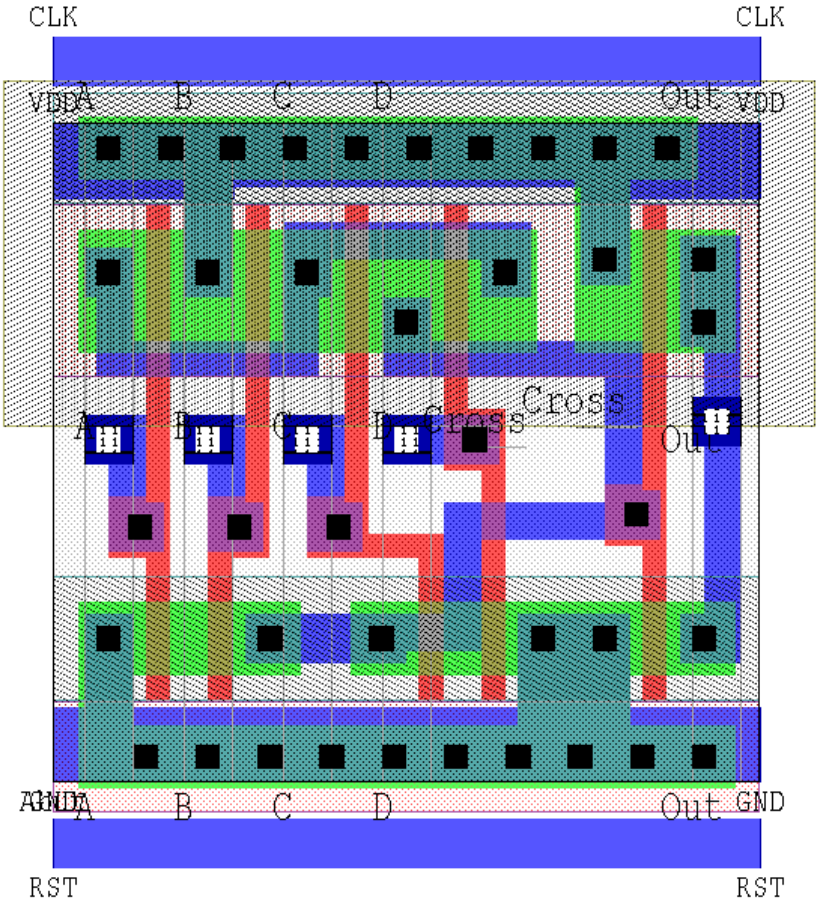
Logic Equation

$$Out = (A \times B) + (C \times D)$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

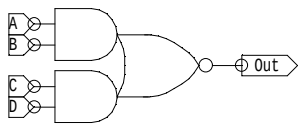
$Tpd0 \rightarrow 1.....135 + 780 \times C[OUT]$
$Tpd1 \rightarrow 0.....92 + 790 \times C[OUT]$



Description: 2 X 2 Input AND-NOR Gate

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	AOI22
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	AOI22
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A*B	C*D	Out
0	0	1
1	X	0
X	1	0

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953
D	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	41 λ	2173 λ^2	2	1X

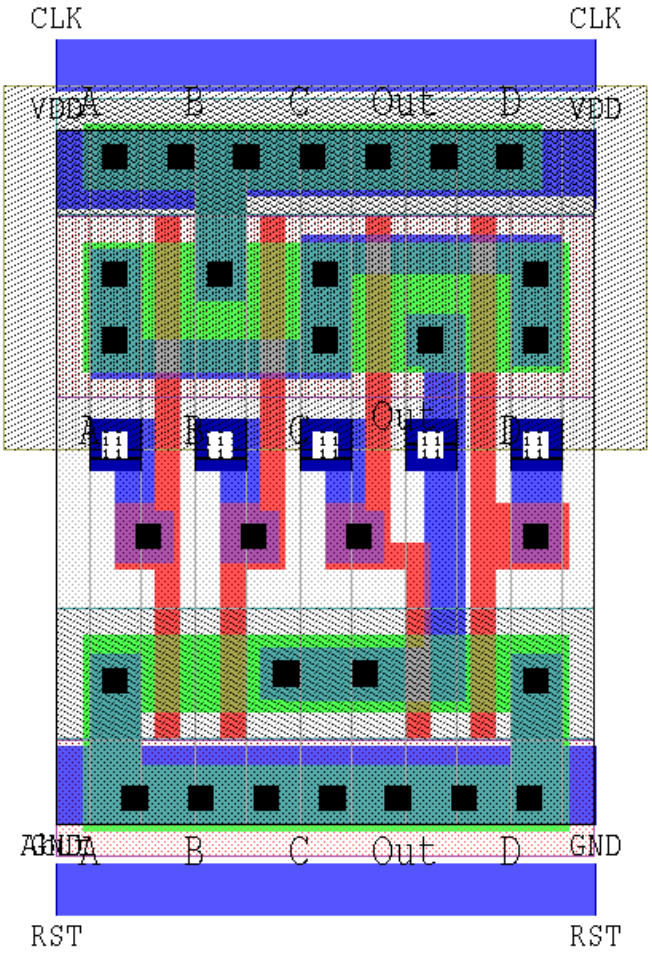
Logic Equation

$$Out = \overline{(A \times B) + (C \times D)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

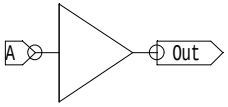
$Tpd0 \rightarrow 1.....60 + 822 \times C[OUT]$
$Tpd1 \rightarrow 0.....97 + 1084 \times C[OUT]$



Non-Inverting Buffer — BUF1

Description: Non-Inverting Buffer

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	Buf1
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	Buf1
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	A | Out 0 | 0 1 | 1	| Ci(fF) A | 6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	25 λ	1325 λ^2	1	1X

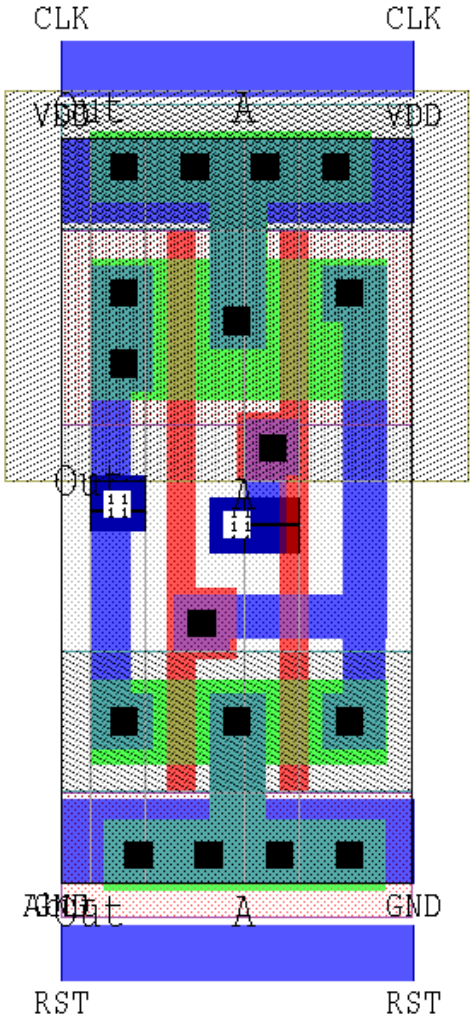
Logic Equation

Out = A

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$Tpd0 \rightarrow 1.....31 + 537 \times C[OUT]$
$Tpd1 \rightarrow 0.....31 + 567 \times C[OUT]$

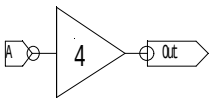


4X-Drive Buffer — BUF4

Description: 4X-Non-Inverting Buffer

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUF4
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUF4
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance



A	Out
0	0
1	1

	Ci(fF)
A	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	50 λ	2650 λ^2	2.5	4X

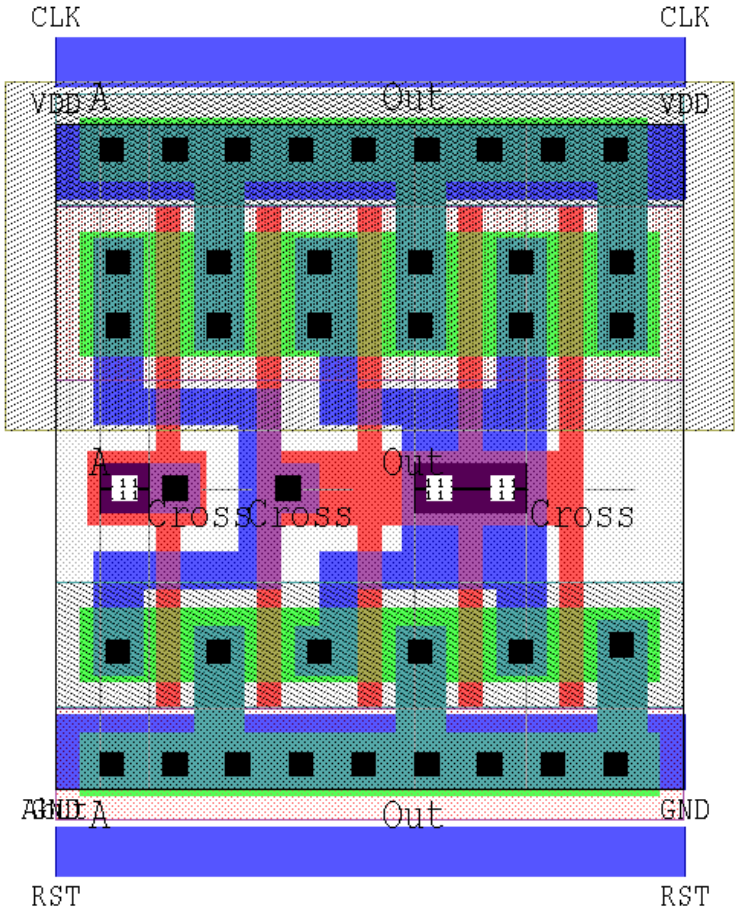
Logic Equation

Out = A

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

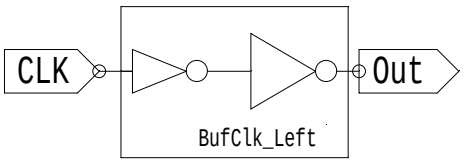
Tpd0 → 1.....49 + 156 × C[OUT]
Tpd1 → 0.....49 + 167 × C[OUT]



Buffer Clock Left — BUFCLKL

Description: Buffer Clock Left

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUFCLKL
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUFCLKL
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

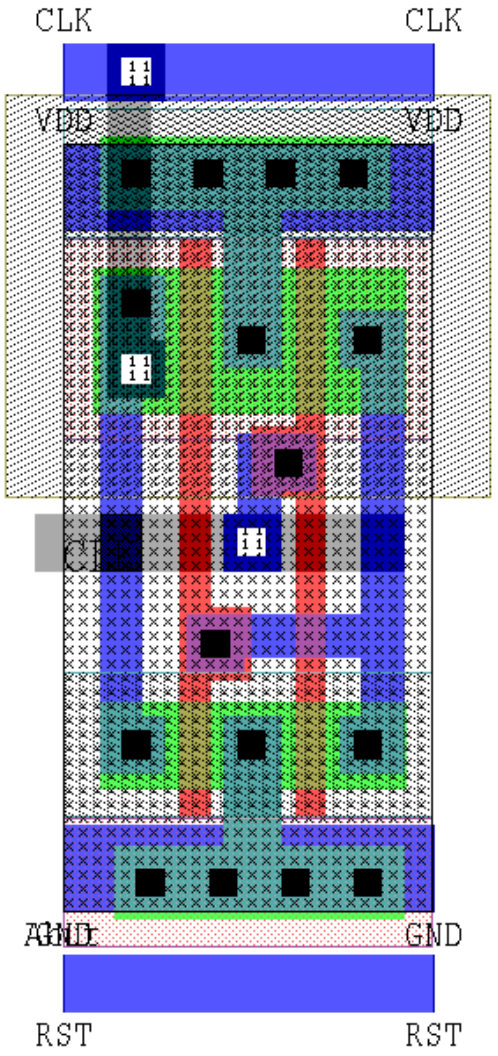
CLK	OUT
0	0
1	1

Height	Width	Area	Equivalent Gate	Drive
53 λ	25.5 λ	1351.5 λ^2	N/A	N/A

Logic Equation

Out = CLK

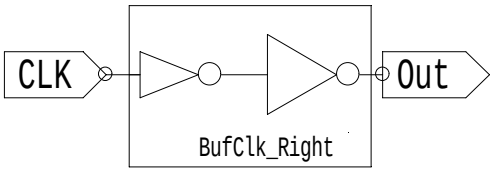
Delay Characteristics: N/A



Buffer Clock Right — BUFCLKR

Description: Buffer Clock Right

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUFCLKR
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUFCLKR
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

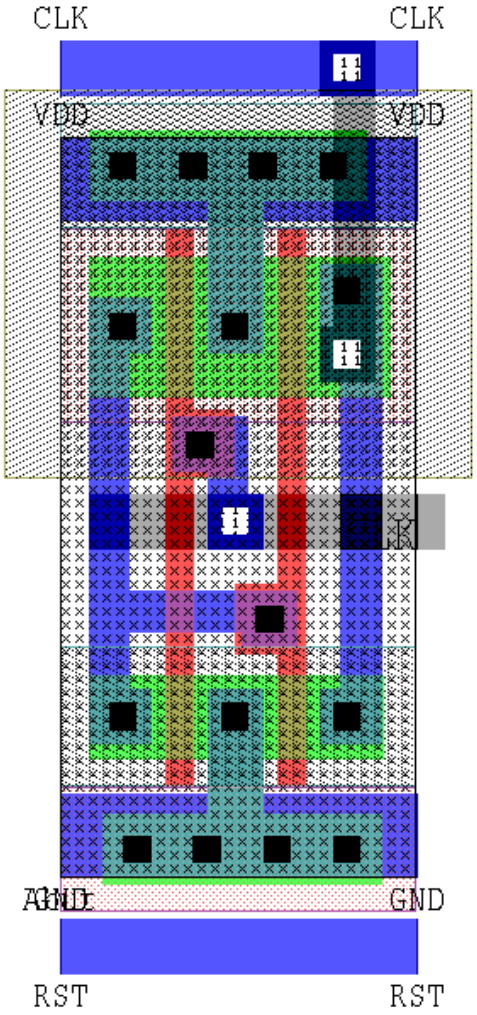
CLK	OUT
0	0
1	1

Height	Width	Area	Equivalent Gate	Drive
53 λ	25.5 λ	1351.5 λ^2	N/A	N/A

Logic Equation

Out = CLK

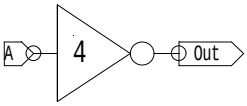
Delay Characteristics: N/A



Description: 4X-Non-Inverting Buffer

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUFI4
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUFI4
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	Out
0	1
1	0

Capacitance

	Ci(fF)
A	27.811

Height	Width	Area	Equivalent Gate	Drive
53 λ	41 λ	2173 λ^2	2	4X

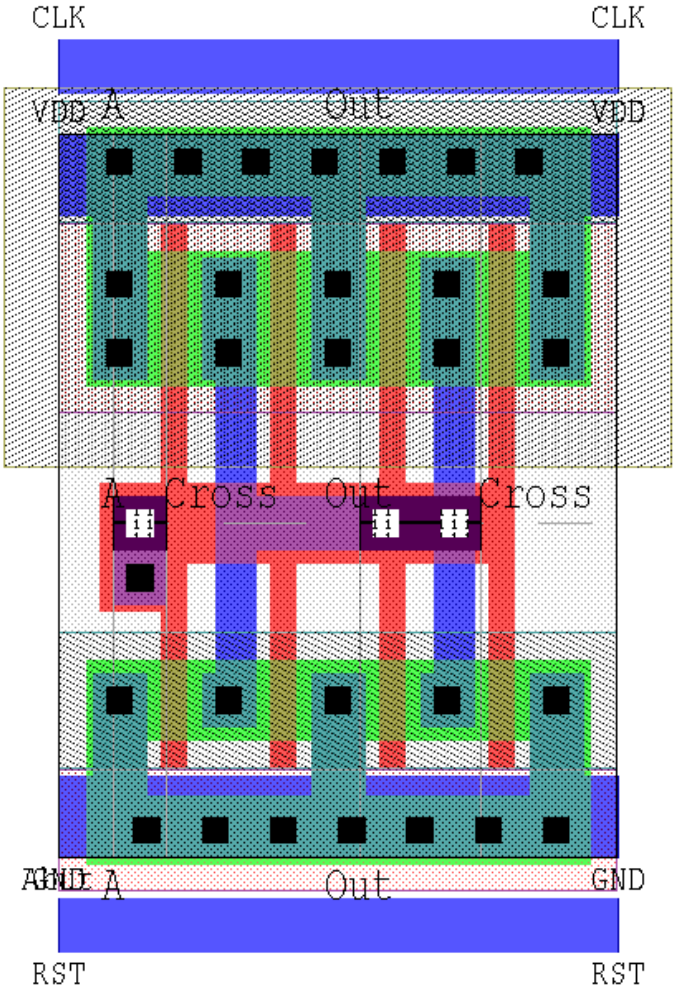
Logic Equation

$\text{Out} = \overline{A}$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

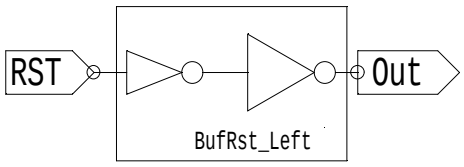
$\text{Tpd0} \rightarrow 1.....14 + 138 \times \text{C[OUT]}$
$\text{Tpd1} \rightarrow 0.....16 + 141 \times \text{C[OUT]}$



Buffer Reset Left — BUFRSTL

Description: Buffer Reset Left

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUFRSTL
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUFRSTL
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

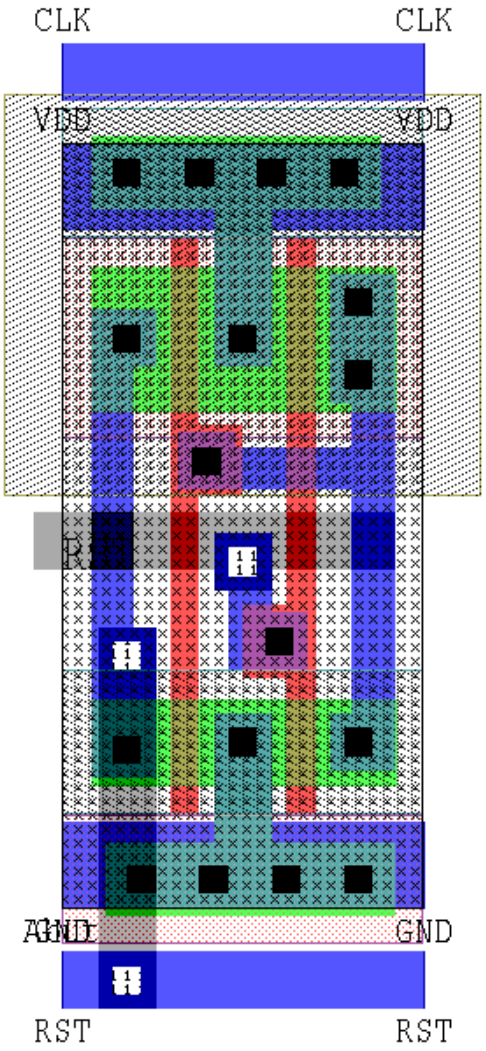
RST	OUT
0	0
1	1

Height	Width	Area	Equivalent Gate	Drive
53 λ	25 λ	1325 λ^2	N/A	N/A

Logic Equation

Out = RST

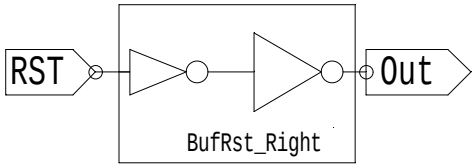
Delay Characteristics: N/A



Buffer Reset Right — BUFRSTR

Description: Buffer Reset Right

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUFRSTR
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUFRSTR
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

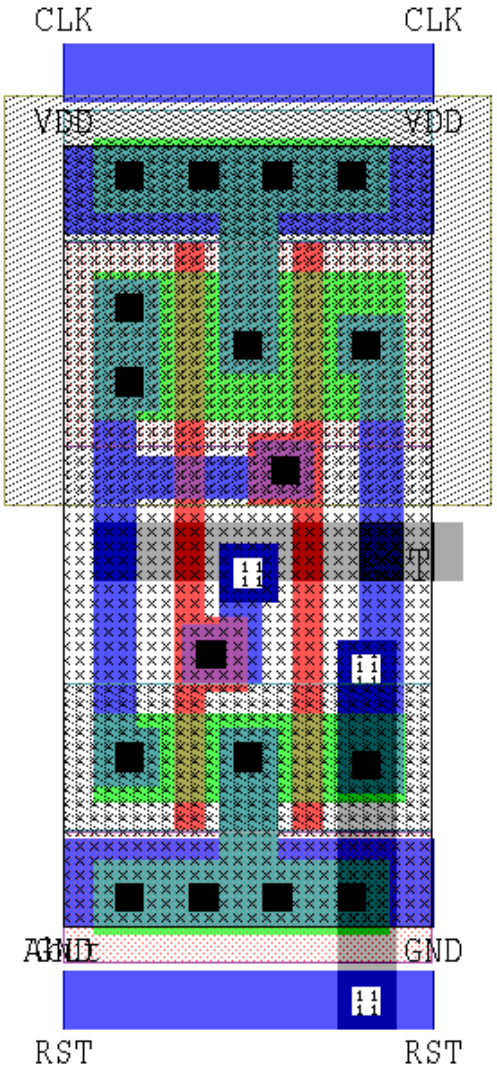
RST	OUT
0	0
1	1

Height	Width	Area	Equivalent Gate	Drive
53 λ	25 λ	1325 λ^2	N/A	N/A

Logic Equation

Out = RST

Delay Characteristics: N/A

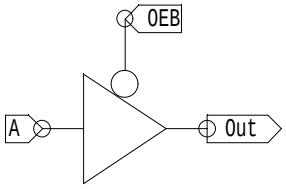


Tri-State Buffer — BUFZ

Description: Tri-State Buffer

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: BUFZ
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: BUFZ
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

OEB	A	Out
1	X	Z
0	0	0
0	1	1

Capacitance

	Ci(fF)
OEB	13.905
A	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	59 λ	3127 λ^2	2.5	1X

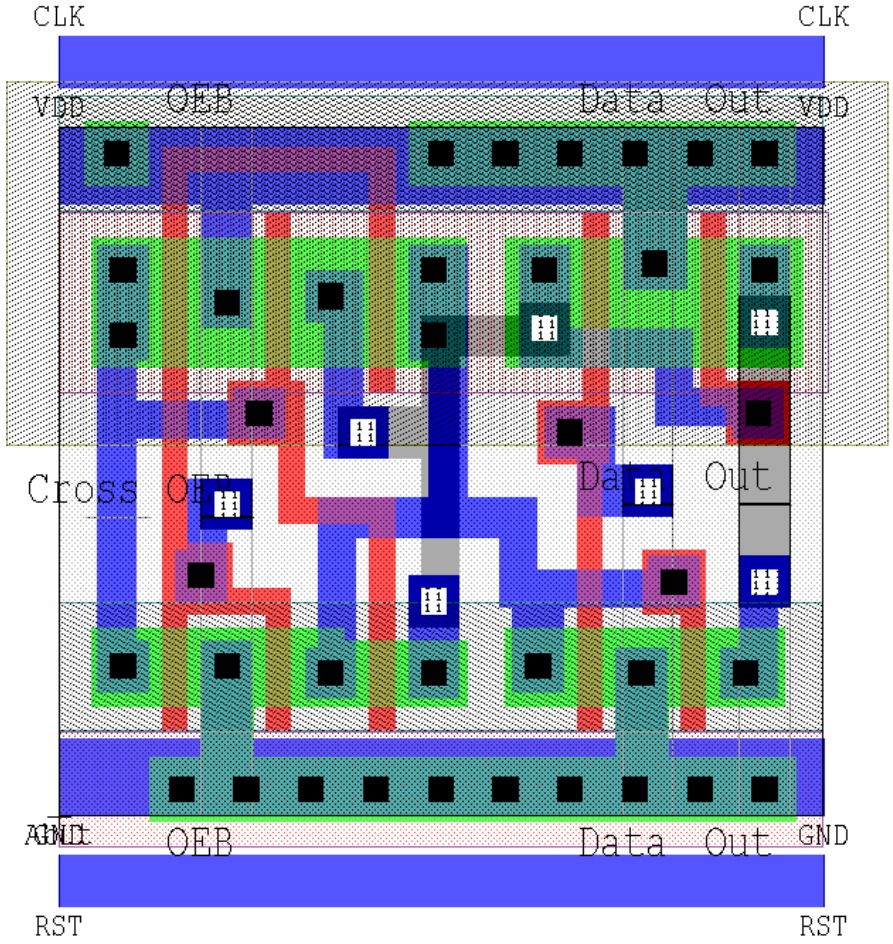
Logic Equation

Out = A

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

Tr.....94 + 805 × C[OUT]
Tf.....89 + 787 × C[OUT]
Tzh.....36 + 87 × C[OUT]
Tzl.....22 + 128 × C[OUT]
Thz.....41 + 7 × C[OUT]
Tlz.....12 + 125 × C[OUT]



Bus Clock Left BUSCLKL

Description: Bus Clock Left

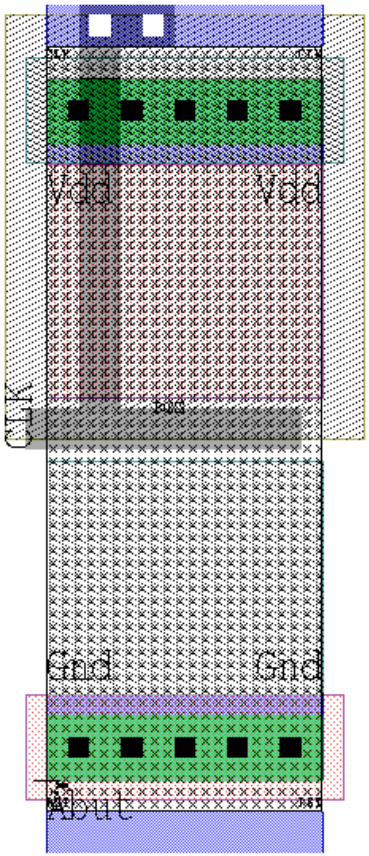
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	BUSCLKL
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	BUSCLKL
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
53 λ	24 λ	1272 λ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A



Bus Clock Right BUSCLKR

Description: Bus Clock Right

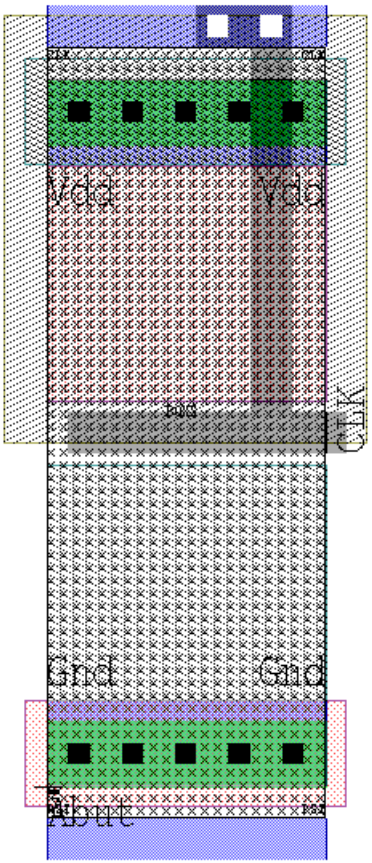
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	BUSCLKR
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	BUSCLKR
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
53 λ	24 λ	1272 λ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A



Bus Reset Left BUSRSTL

Description: Bus Reset Left

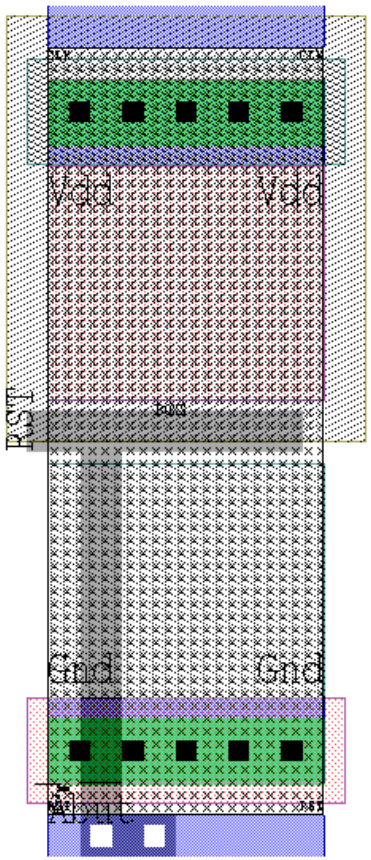
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	BUSRSTL
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	BUSRSTL
Mapping Macros: GateSim:	TannerLb\nettran\scmos\scms2sim.mac	
L-Edit/SPR:	TannerLb\nettran\scmos\scms2tpr.mac	

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
53 λ	24 λ	1272 λ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A



Bus Reset Right BUSRSTR

Description: Bus Reset Right

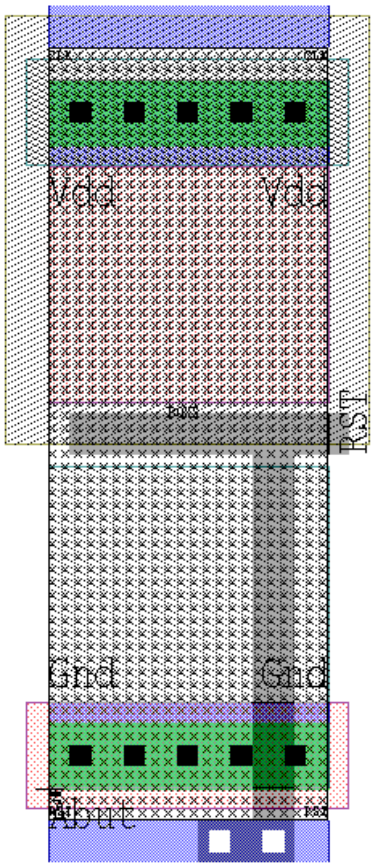
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	BUSRSTR
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	BUSRSTR
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
53 λ	24 λ	1272 λ^2	N/A	N/A

Logic Equation
N/A

Delay Characteristics: N/A

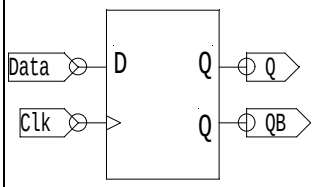


D Flip-Flop — DFF_s

Description: D Flip-Flop

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: DFF_s
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: DFF_s
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

Clk	Data	Q(t+1)	QB(t+1)
1	X	Q(t)	QB(t)
0	X	Q(t)	QB(t)
↑	0	0	1
↑	1	1	0

Capacitance

	Ci(fF)
Clk	6.953
Data	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	154.5 λ	8188.5 λ^2	7	1X

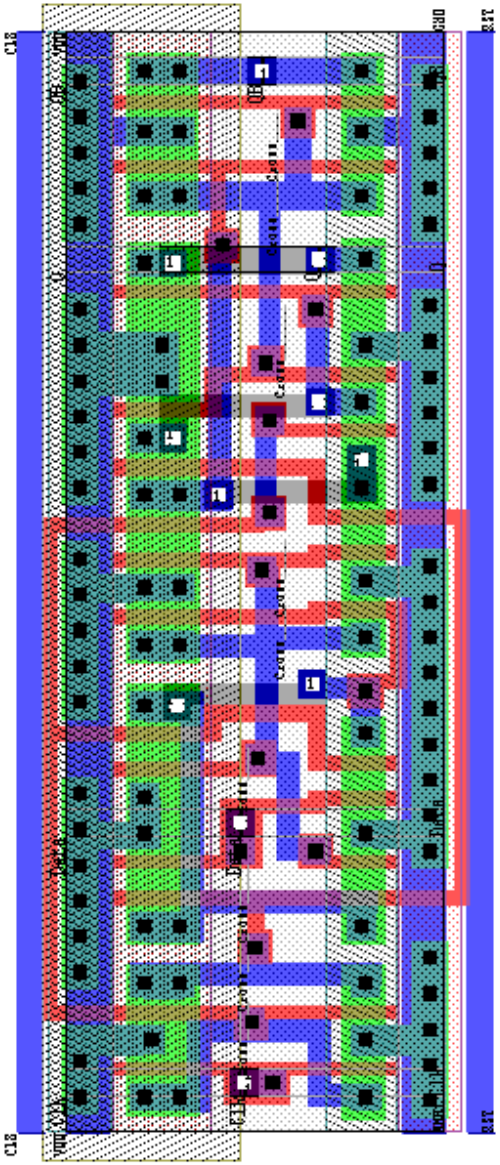
Logic Equation

$$I(t+1) = (Data \times \overline{Clk}) + (I(t) \times Clk)$$
$$Q(t+1) = (I(t) \times Clk) + (Q(t) \times \overline{Clk})$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$T_r Q$.....$179 + 545 \times C[Q]$
$T_f Q$.....$152 + 579 \times C[Q]$
$T_r QB$.....$122 + 555 \times C[QB]$
$T_f QB$.....$150 + 595 \times C[QB]$

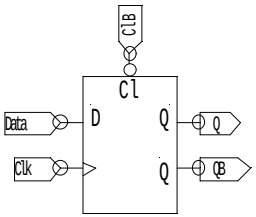


D Flip-Flop AC — DFFC_s

Description: D Flip-Flop with Asynchronous Clear

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: DFFC_s
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: DFFC_s
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

Clk	ClB	Data	Q(t+1)	QB(t+1)
X	0	X	0	1
1	1	X	Q(t)	QB(t)
0	1	X	Q(t)	QB(t)
↑	1	0	0	1
↑	1	1	1	0

Capacitance

	Ci(fF)
Clk	6.953
ClB	13.905
Data	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	197 λ	10441 λ^2	8.5	1X

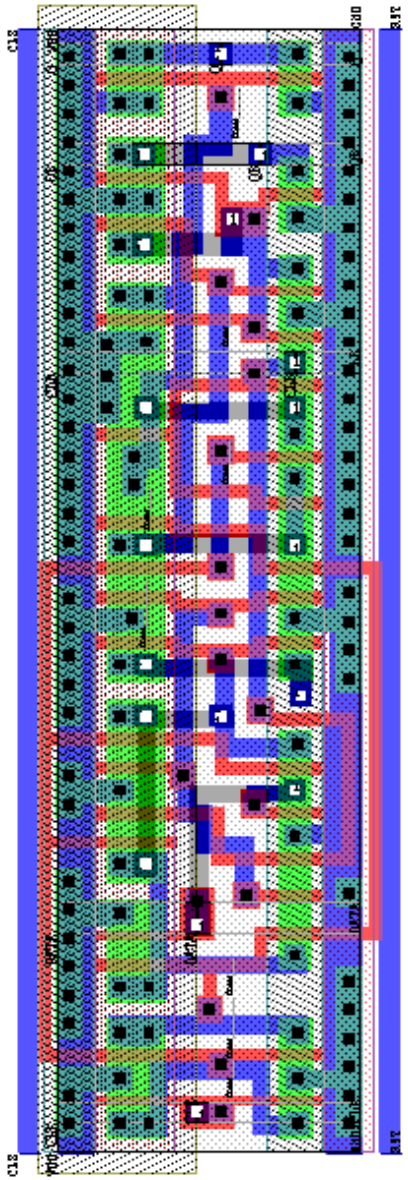
Logic Equation

$$I(t+1) = (Data \times \overline{Clk}) + (I(t) \times Clk) \times \overline{ClB}$$
$$Q(t+1) = (I(t) \times Clk) + (Q(t) \times \overline{Clk}) \times \overline{ClB}$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

T_rQ..... $283 + 990 \times C[Q]$
T_fQ..... $104 + 828 \times C[Q]$
$T_{rst}Q$..... $87 + 920 \times C[Q]$
T_rQB..... $115 + 630 \times C[QB]$
T_fQB..... $168 + 611 \times C[QB]$
$T_{rst}QB$..... $135 + 549 \times C[QB]$

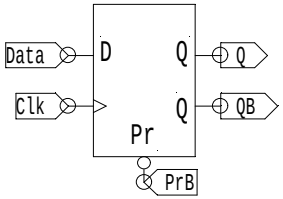


D Flip-Flop Preset — DFFP_s

Description: D Flip-Flop with Preset

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: DFFP_s
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: DFFP_s
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

Clk	PrB	Data	Q(t+1)	QB(t+1)
X	0	X	1	0
1	1	X	Q(t)	QB(t)
0	1	X	Q(t)	QB(t)
↑	1	0	0	1
↑	1	1	1	0

Capacitance

	Ci(fF)
Clk	6.953
PrB	13.905
Data	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	175.5 λ	9301.5 λ^2	8	1X

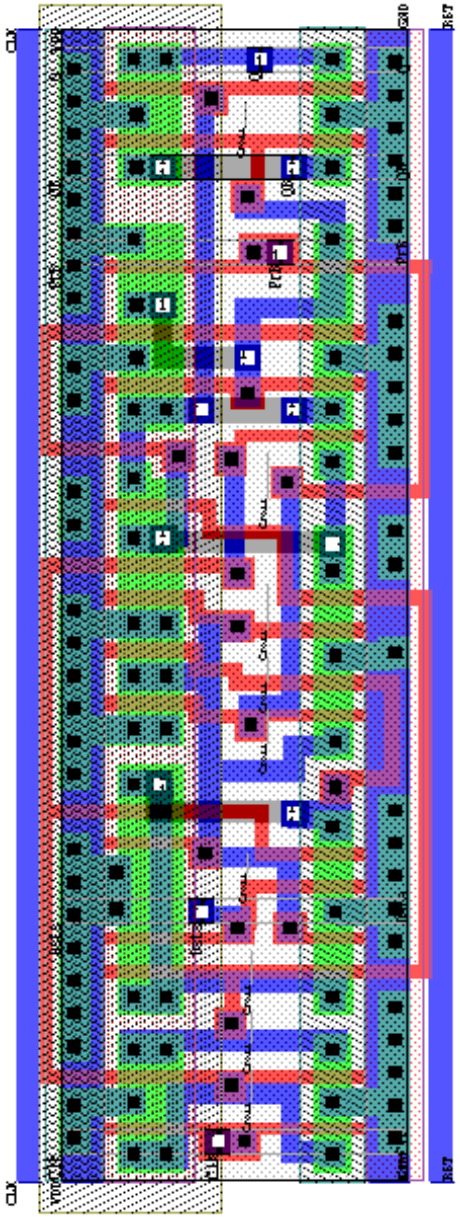
Logic Equation

$$I(t+1) = (Data \times \overline{Clk}) + (I(t) \times Clk) \times \overline{PrB}$$
$$Q(t+1) = (I(t) \times Clk) + (Q(t) \times \overline{Clk}) \times \overline{PrB}$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

T_rQ..... $219 + 571 \times C[Q]$
T_fQ..... $208 + 624 \times C[Q]$
$T_{set}Q$..... $103 + 732 \times C[Q]$
T_rQB..... $166 + 675 \times C[QB]$
T_fQB..... $179 + 631 \times C[QB]$
$T_{set}QB$..... $41 + 610 \times C[QB]$

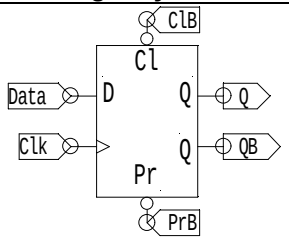


D Flip-Flop P/AC — DFFPC_s

Description: D Flip-Flop with Preset and Asynchronous Clear

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	DFFPC_s
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	DFFPC_s
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

Clk	PrB	ClB	Data	Q(t+1)	QB(t+1)
X	0	1	X	1	0
X	1	0	X	0	1
X	0	0	X	1	1
X	↑	↑	X	?	?
1	1	1	X	Q(t)	QB(t)
0	1	1	X	Q(t)	QB(t)
↑	1	1	0	0	1
↑	1	1	1	1	0

Capacitance

	Ci(fF)
Clk	6.953
PrB	13.905
ClB	13.905
Data	6.953

? Indeterminate value

Height	Width	Area	Equivalent Gate	Drive
53 λ	217 λ	11501 λ^2	9.5	1X

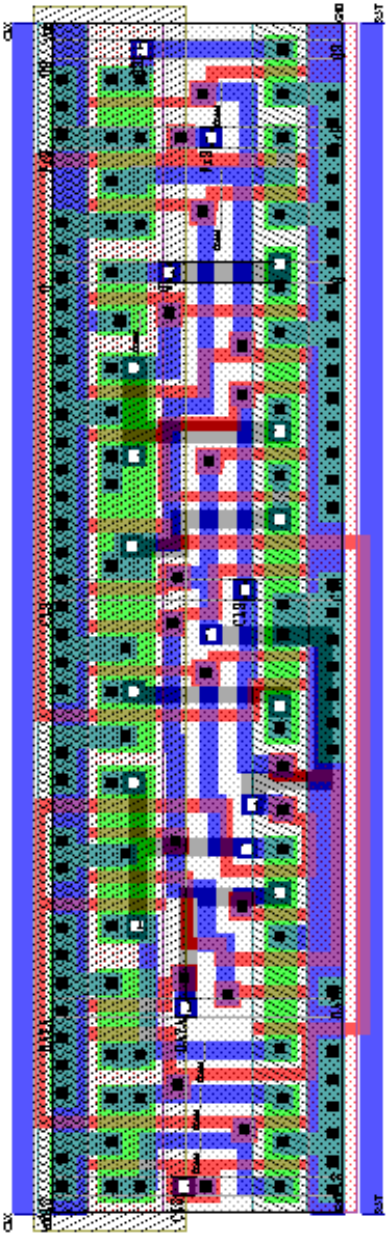
Logic Equation

$$I(t+1) = (Data \times \overline{Clk}) + (I(t) \times Clk) \times \overline{ClB} \times \overline{PrB}$$
$$Q(t+1) = (I(t) \times Clk) + (Q(t) \times \overline{Clk}) \times \overline{ClB} \times \overline{PrB}$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

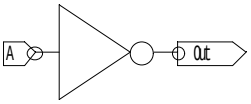
T_rQ.....$323 + 843 \times C[Q]$
T_fQ.....$233 + 713 \times C[Q]$
$T_{set}Q$.....$159 + 847 \times C[Q]$
$T_{rst}Q$.....$83 + 843 \times C[Q]$
T_rQB.....$160 + 655 \times C[QB]$
T_fQB.....$208 + 622 \times C[QB]$
$T_{set}QB$.....$39 + 594 \times C[QB]$
$T_{rst}QB$.....$168 + 653 \times C[QB]$



Description: Inverter

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: INV
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: INV
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance



A	Out
0	1
1	0

	Ci(fF)
A	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	18 λ	954 λ^2	0.5	1X

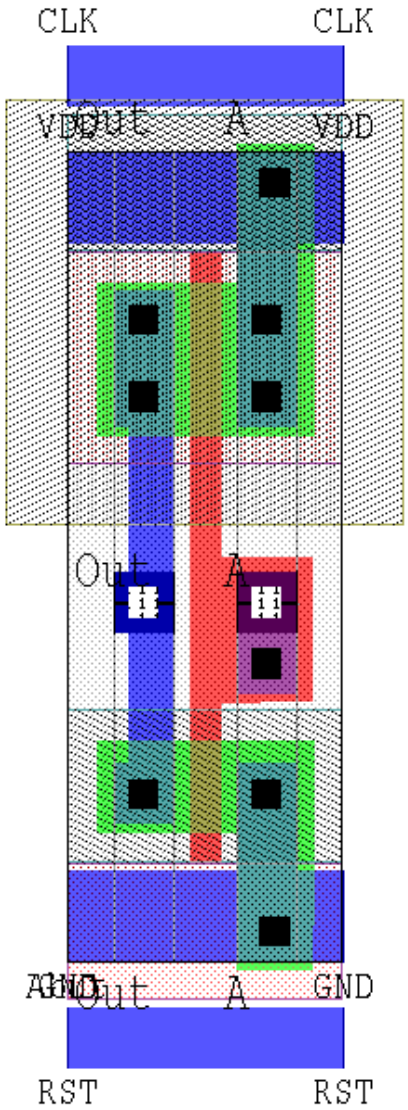
Logic Equation

$\text{Out} = \overline{A}$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$\text{Tpd0} \rightarrow 1 \ldots\ldots\ldots 12 + 529 \times \text{C[OUT]}$
$\text{Tpd1} \rightarrow 0 \ldots\ldots\ldots 12 + 549 \times \text{C[OUT]}$

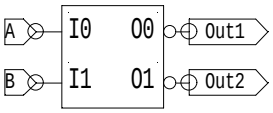


Dual Inverter — INV2

Description: Dual Inverter

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: INV2
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: INV2
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out1	Out2
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

Capacitance

	Ci(fF)
A	6.953
B	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	33 λ	1749 λ^2	1	1X

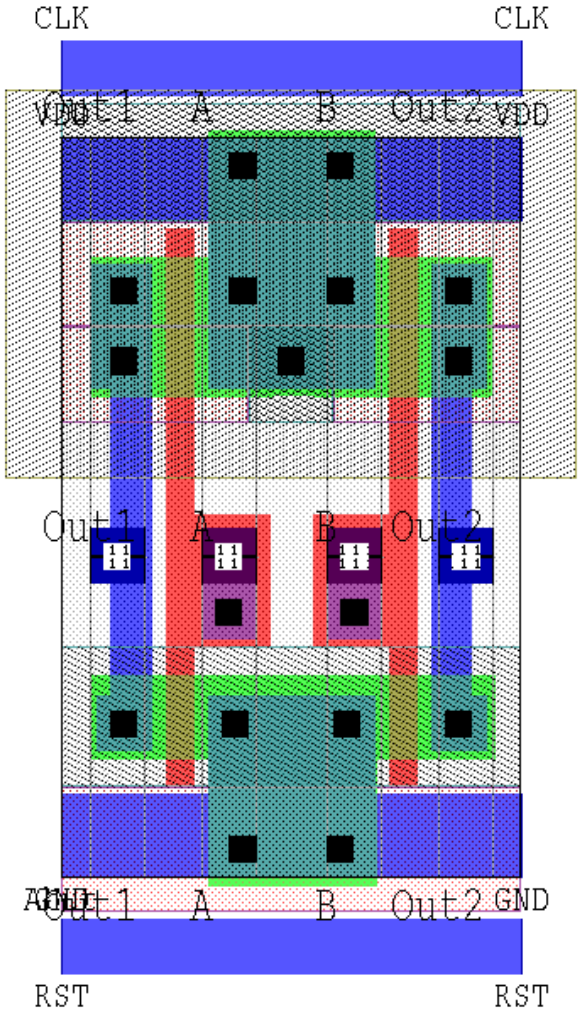
Logic Equation

$Out1 = \overline{A}$
$Out2 = \overline{B}$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$Tpd0 \rightarrow 1 \ldots\ldots\ldots 11 + 529 \times C[OUT1]$
$Tpd1 \rightarrow 0 \ldots\ldots\ldots 12 + 539 \times C[OUT1]$
$Tpd0 \rightarrow 1 \ldots\ldots\ldots 14 + 538 \times C[OUT2]$
$Tpd1 \rightarrow 0 \ldots\ldots\ldots 14 + 500 \times C[OUT2]$

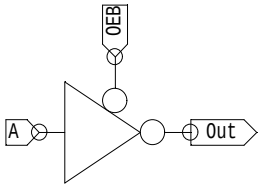


Tri-State Inverter — INVZ

Description: Tri-State Inverter

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: INVZ
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: INVZ
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

OEB	A	Out
1	X	Z
0	0	1
0	1	0

Capacitance

	Ci(fF)
OEB	13.905
A	13.905

Height	Width	Area	Equivalent Gate	Drive
53 λ	43 λ	2279 λ^2	2.5	1X

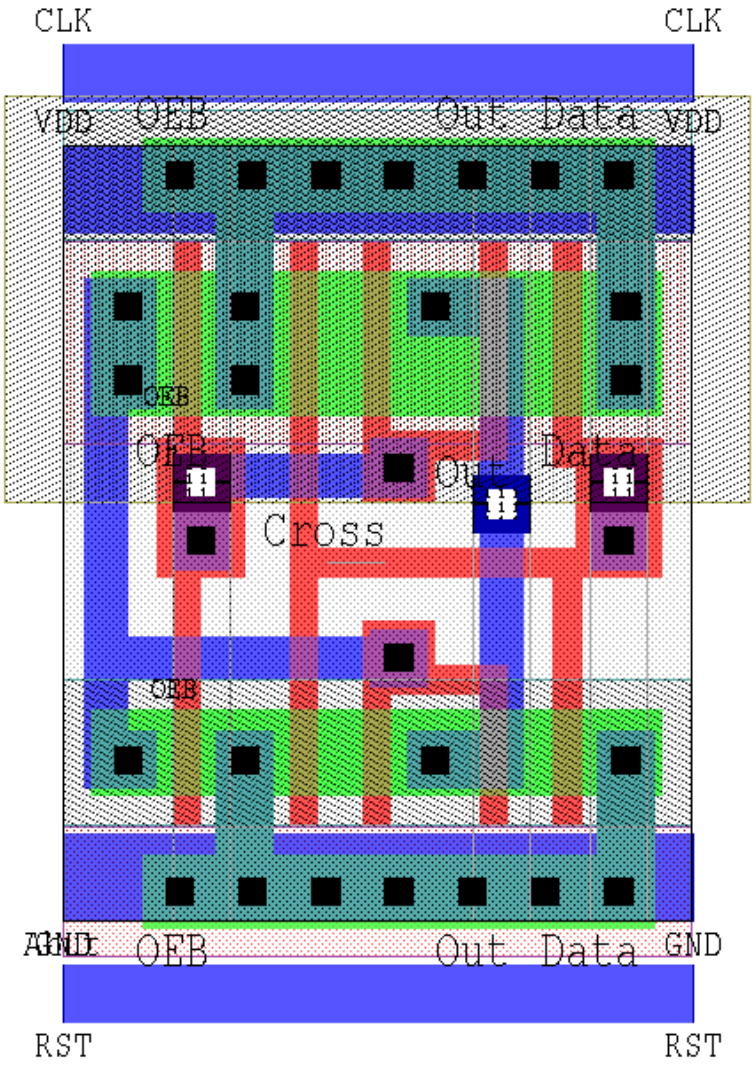
Logic Equation

$Out = \overline{A}$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

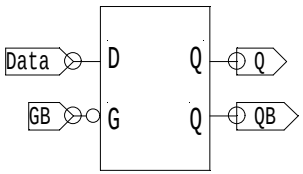
Tr.....25 + 534 × C[OUT]
Tf.....27 + 521 × C[OUT]
Tzh.....1
Tzl.....16 + 36 × C[OUT]
Thz.....1
Tlz.....17



Description: Latch

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: LAT
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: LAT
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

GB	Data	Q(t+1)	QB(t+1)
0	0	0	1
0	1	1	0
1	X	Q(t)	QB(t)

Capacitance

	Ci(fF)
GB	6.953
Data	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	79 λ	4187 λ^2	3.5	1X

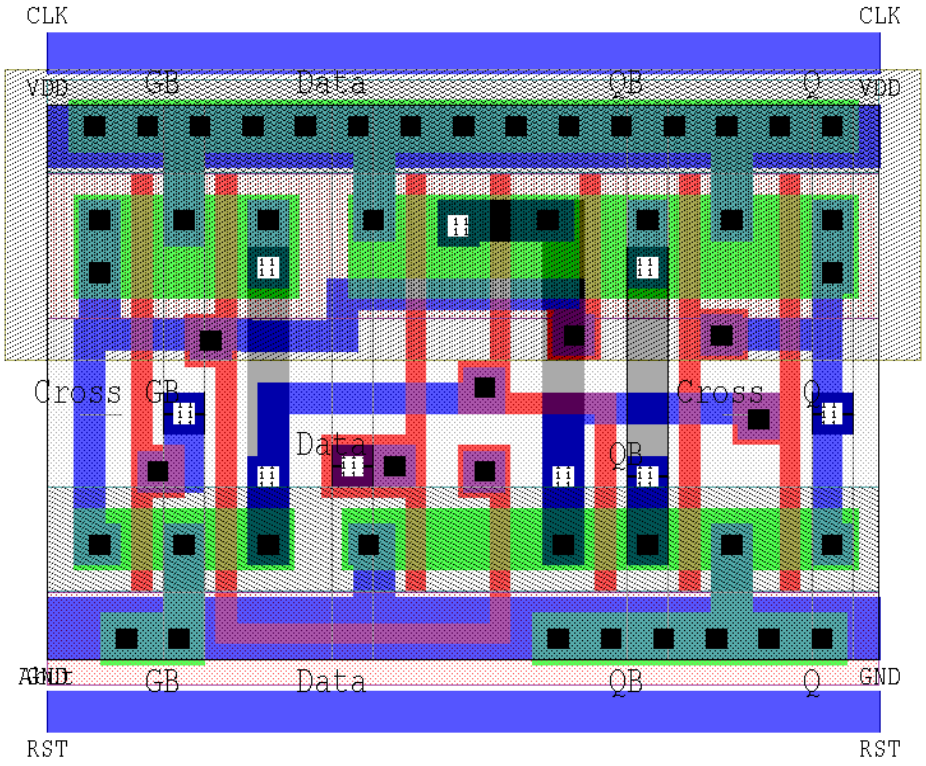
Logic Equation

$$Q(t+1) = (Data \times \overline{GB}) + (Q(t) \times GB)$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

T_r DQ.....86 + 652 × C[Q]
T_f DQ.....85 + 697 × C[Q]
T_r GQ.....118 + 699 × C[Q]
T_f GQ.....105 + 650 × C[Q]
T_r DQB.....110 + 1531 × C[QB]
T_f DQB.....114 + 1512 × C[QB]
T_r GQB.....143 + 1532 × C[QB]
T_f GQB.....132 + 1512 × C[QB]

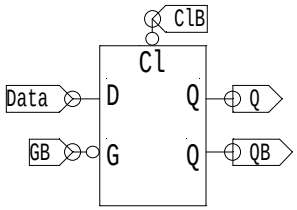


Latch with Clear — LATC

Description: Latch with Clear

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: LATC
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: LATC
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

GB	ClB	Data	Q(t+1)	QB(t+1)
X	0	X	0	1
0	1	0	0	1
0	1	1	1	0
1	1	X	Q(t)	QB(t)

Capacitance

	Ci(fF)
GB	6.953
ClB	6.953
Data	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	96 λ	5088 λ^2	4.5	1X

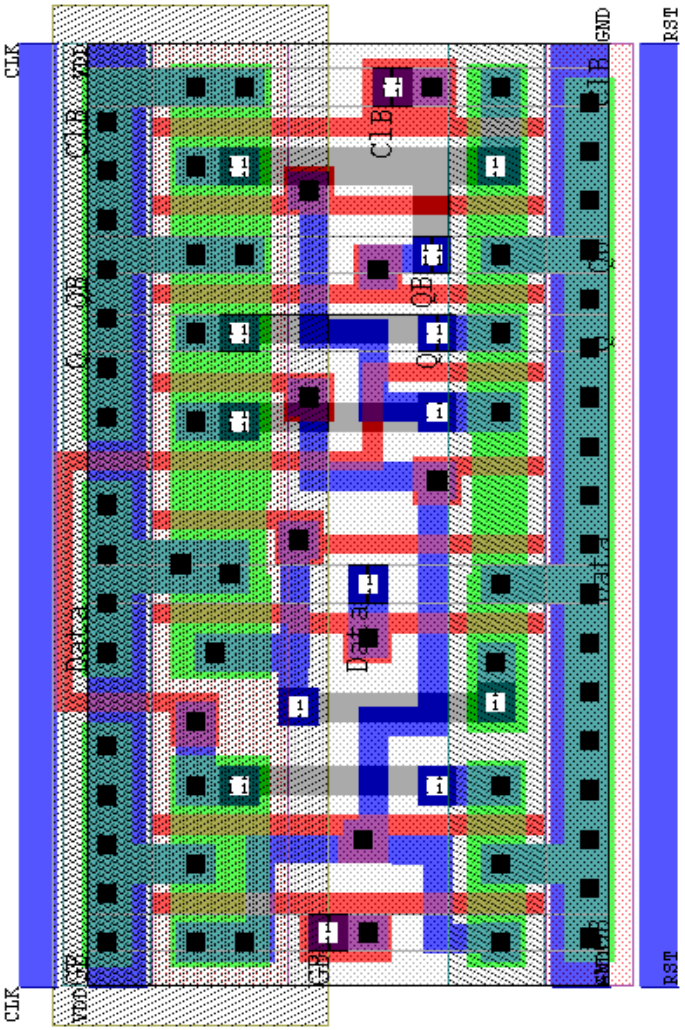
Logic Equation

$$Q(t+1) = (\text{Data} \times \overline{GB}) + (Q(t) \times GB) \times ClB$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

T_r DQ.....$150 + 2053 \times C[Q]$
T_f DQ.....$149 + 1493 \times C[Q]$
T_r GQ.....$144 + 1489 \times C[Q]$
T_f GQ.....$162 + 2053 \times C[Q]$
T_{rst} Q.....$40 + 1419 \times C[Q]$
T_r DQB.....$120 + 628 \times C[QB]$
T_f DQB.....$121 + 1027 \times C[QB]$
T_r GQB.....$115 + 626 \times C[QB]$
T_f GQB.....$132 + 1029 \times C[QB]$
T_{rst} QB.....$15 + 531 \times C[QB]$

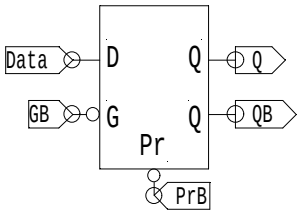


Latch with Preset — LATP

Description: Latch with Preset

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: LATP
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: LATP
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

GB	PrB	Data	Q(t+1)	QB(t+1)
X	0	X	1	0
0	1	0	0	1
0	1	1	1	0
1	1	X	Q(t)	QB(t)

Capacitance

	Ci(fF)
GB	6.953
PrB	6.953
Data	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	87 λ	4611 λ^2	4	1X

Logic Equation

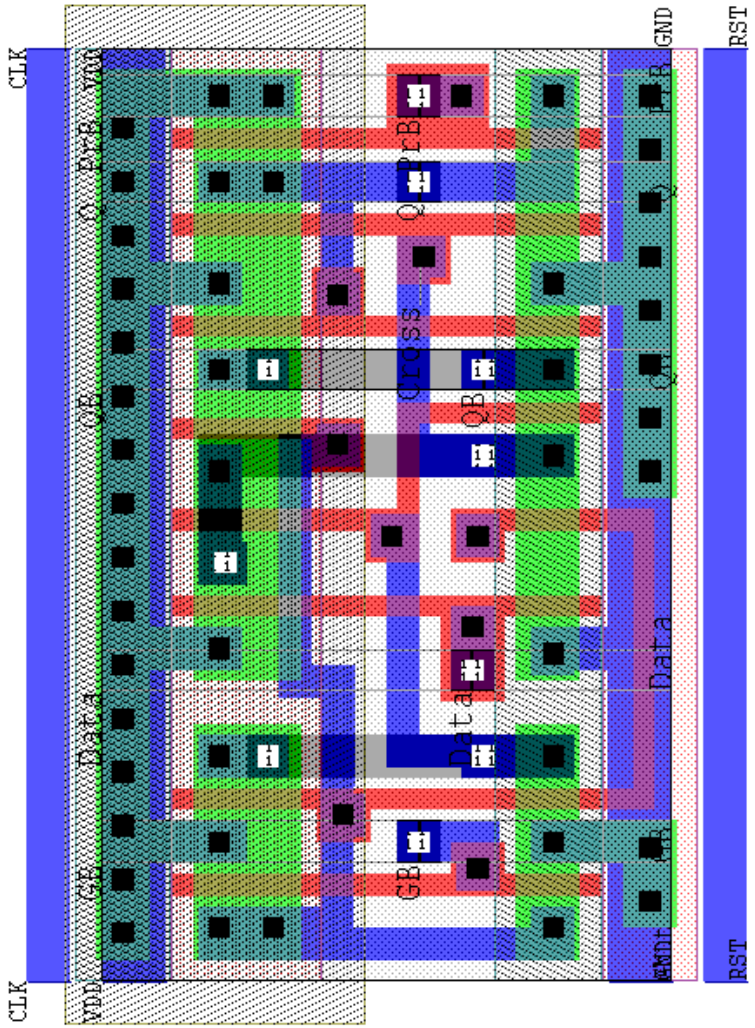
$$Q(t+1) = (Data \times \overline{GB}) + ((Q(t) \times GB) + \overline{PrB})$$

$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

T_r DQ.....$97 + 624 \times C[Q]$
T_f DQ.....$102 + 1029 \times C[Q]$
T_r GQ.....$135 + 1038 \times C[Q]$
T_f GQ.....$116 + 623 \times C[Q]$
T_{set}Q.....$16 + 523 \times C[Q]$
T_r DQB.....$132 + 2053 \times C[QB]$
T_f DQB.....$126 + 1489 \times C[QB]$
T_r GQB.....$166 + 2053 \times C[QB]$
T_f GQB.....$145 + 1487 \times C[QB]$
T_{set}QB.....$42 + 1417 \times C[QB]$

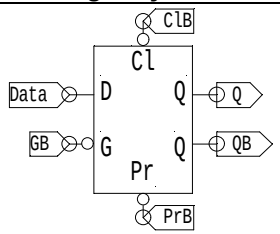


Latch with Pre/Clr — LATPC

Description: Latch with Preset and Clear

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: LATPC
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: LATPC
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

GB	PrB	ClB	Data	Q(t+1)	QB(t+1)
X	0	X	1	1	0
X	1	0	X	0	1
1	↑	↑	X	?	?
0	1	1	0	0	1
0	1	1	1	1	0
1	1	1	X	Q(t)	QB(t)

Capacitance

	Ci(fF)
GB	6.953
PrB	6.953
ClB	6.953
Data	6.953

? Indeterminate value

Height	Width	Area	Equivalent Gate	Drive
53 λ	116 λ	6148 λ^2	5	1X

Logic Equation

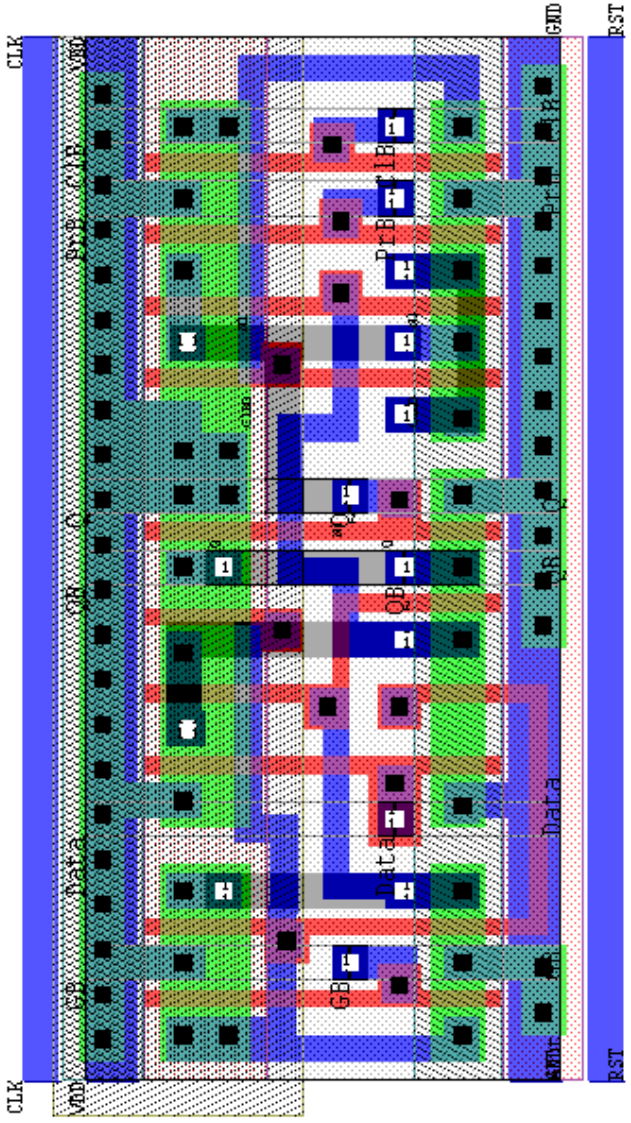
$$Q(t+1) = \left(\left(Data \times \overline{GB}\right) + \left(Q(t) \times GB\right) \times ClB\right) \times \overline{PrB}$$
$$QB(t+1) = \overline{Q(t+1)}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

T_r DQ.....109 + 1087 × C[Q]
T_f DQ.....108 + 1050 × C[Q]
T_r GQ.....139 + 1050 × C[Q]
T_f GQ.....125 + 1084 × C[Q]
T_{set}Q.....23 + 565 × C[Q]
T_{rst}Q.....763 + 1018 × C[Q]

T_r DQB.....140 + 2086 × C[QB]
T_f DQB.....144 + 2159 × C[QB]
T_r GQB.....171 + 2086 × C[QB]
T_f GQB.....159 + 2157 × C[QB]
T_{set}QB.....54 + 1442 × C[QB]
T_{rst}QB.....97 + 2061 × C[QB]

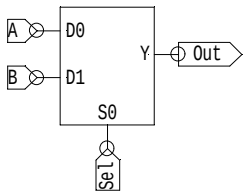


2-Input Multiplexer — MUX2

Description: 2-Input Multiplexer

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	MUX2
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	MUX2
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

Sel	Out
0	B
1	A

Capacitance

	Ci(fF)
A	6.953
B	6.953
Sel	13.905

Height	Width	Area	Equivalent Gate	Drive
53 λ	61 λ	3233 λ^2	3	1X

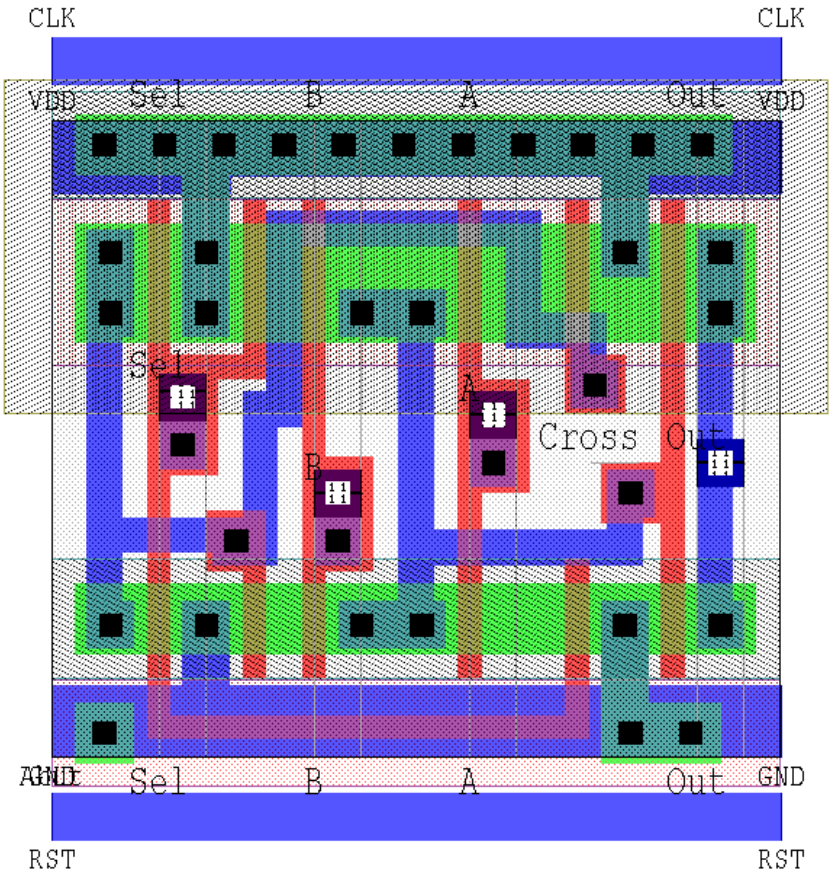
Logic Equation

$$Out = (A \times Sel) + (B \times \overline{Sel})$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

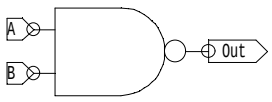
Tpd0→1 A.....$84 + 700 \times C[OUT]$
Tpd1→0 A.....$72 + 821 \times C[OUT]$
Tpd0→1 B.....$91 + 710 \times C[OUT]$
Tpd1→0 B.....$76 + 857 \times C[OUT]$
Tpd0→1 Sel.....$92 + 702 \times C[OUT]$
Tpd1→0 Sel.....$95 + 757 \times C[OUT]$



Description: 2-Input NAND Gate

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NAND2
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NAND2
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out
0	X	1
X	0	1
1	1	0

Capacitance

	Ci(fF)
A	6.953
B	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	26 λ	1378 λ^2	1	1X

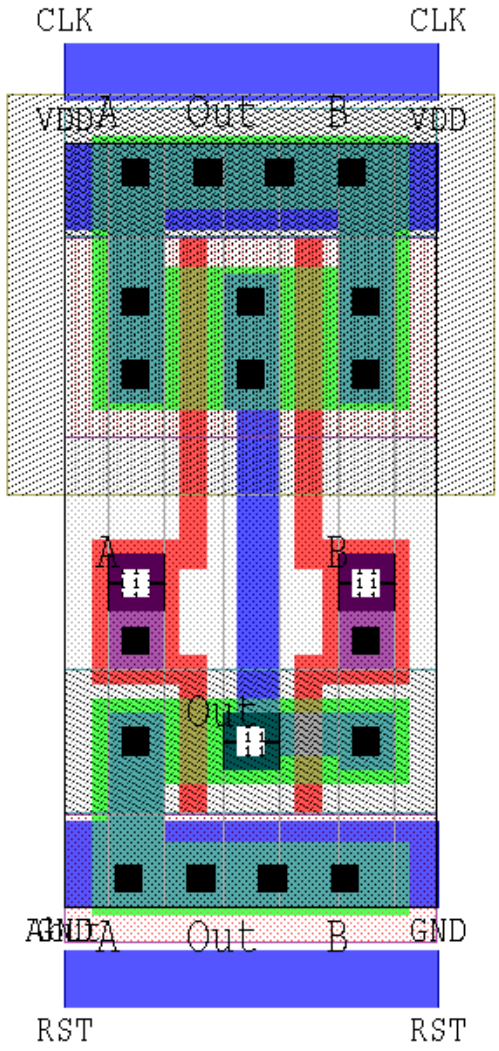
Logic Equation

$Out = \overline{A \; X \; B}$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$Tpd0 \rightarrow 1 \ldots\ldots\ldots 18 + 545 \times C[OUT]$
$Tpd1 \rightarrow 0 \ldots\ldots\ldots 19 + 1159 \times C[OUT]$

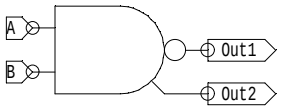


2-Input NAND / AND — NAND2C

Description: 2-Input NAND Gate with Complementary Output

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NAND2C
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NAND2C
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out1	Out2
0	X	1	0
X	0	1	0
1	1	0	1

Capacitance

	Ci(fF)
A	6.953
B	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	38 λ	2014 λ^2	1.5	1X

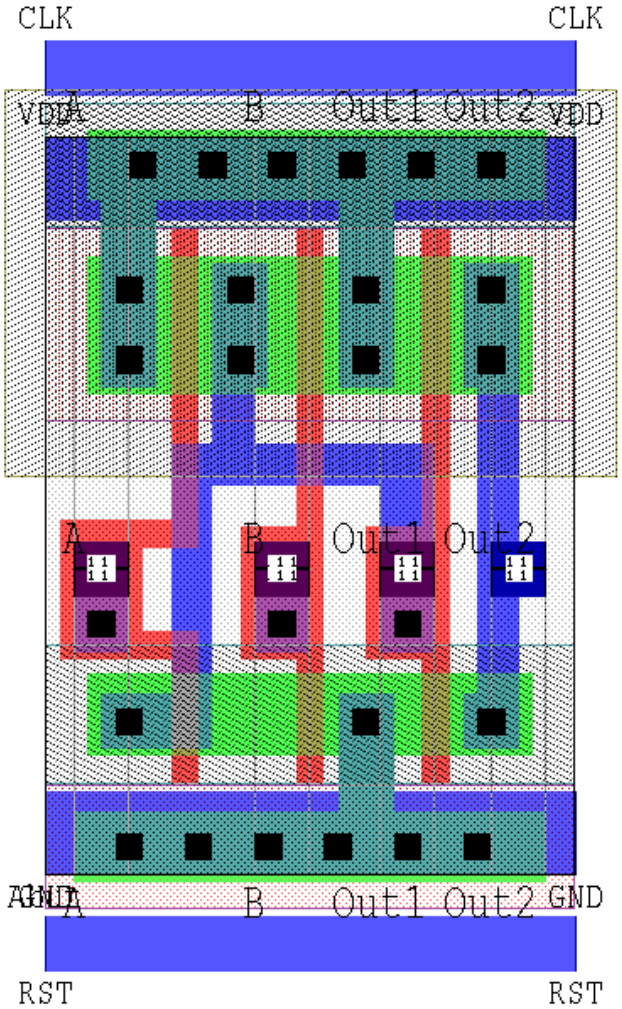
Logic Equation

$Out1 = \overline{A \times B}$
$Out2 = A \times B$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

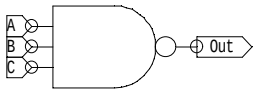
Tpd0→1 NAND.....23 + 543 × C[OUT1]
Tpd1→0 NAND.....34 + 989 × C[OUT1]
Tpd0→1 AND.....56 + 989 × C[OUT1] + 1042 × C[OUT2]
Tpd1→0 AND.....43 + 543 × C[OUT1] + 888 × C[OUT2]



Description: 3-Input NAND Gate

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NAND3
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NAND3
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	Out
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	34 λ	1802 λ^2	1.5	1X

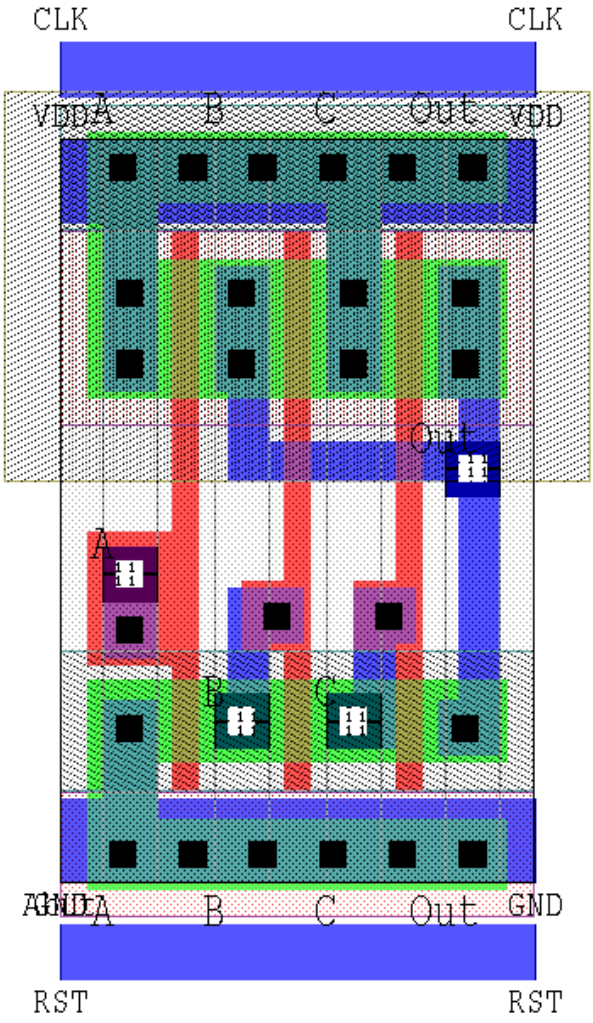
Logic Equation

$$Out = \overline{A \times B \times C}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

Tpd0 → 1.....33 + 554 × C[OUT]
Tpd1 → 0.....83 + 1415 × C[OUT]

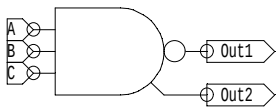


3-Input NAND / AND — NAND3C

Description: 3-Input NAND Gate with Complementary Output

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	NAND3C
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	NAND3C
Mapping Macros: GateSim:	TannerLb\nettran\scmos\scms2sim.mac	
L-Edit/SPR:	TannerLb\nettran\scmos\scms2tpr.mac	

Logic Symbol



Truth Table

A	B	C	Out1	Out2
0	X	X	1	0
X	0	X	1	0
X	X	0	1	0
1	1	1	0	1

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	48 λ	2544 λ^2	2	1X

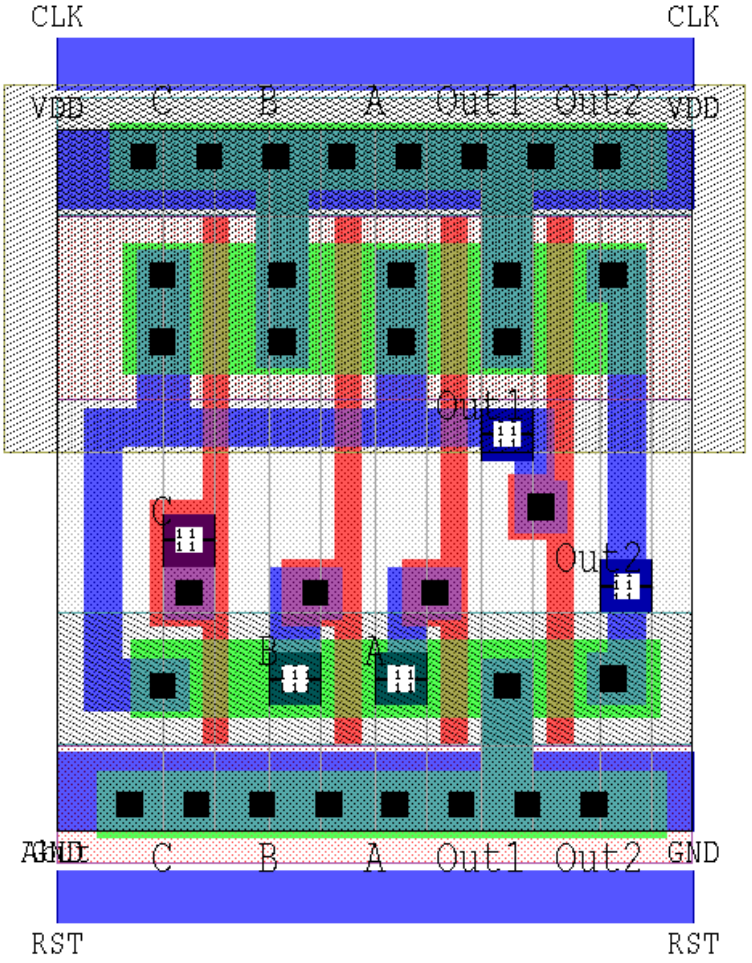
Logic Equation

$$Out1 = \overline{A \times B \times C}$$
$$Out2 = A \times B \times C$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

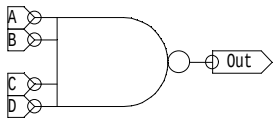
Tpd0 → 1 NAND.....37 + 554 × C[OUT1]
Tpd1 → 0 NAND.....93 + 1413 × C[OUT1]
Tpd0 → 1 AND.....123 + 1413 × C[OUT1] + 1227 × C[OUT2]
Tpd1 → 0 AND.....61 + 554 × C[OUT1] + 919 × C[OUT2]



Description: 4-Input NAND Gate

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NAND4
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NAND4
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	D	Out
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953
D	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	41 λ	2173 λ^2	2	1X

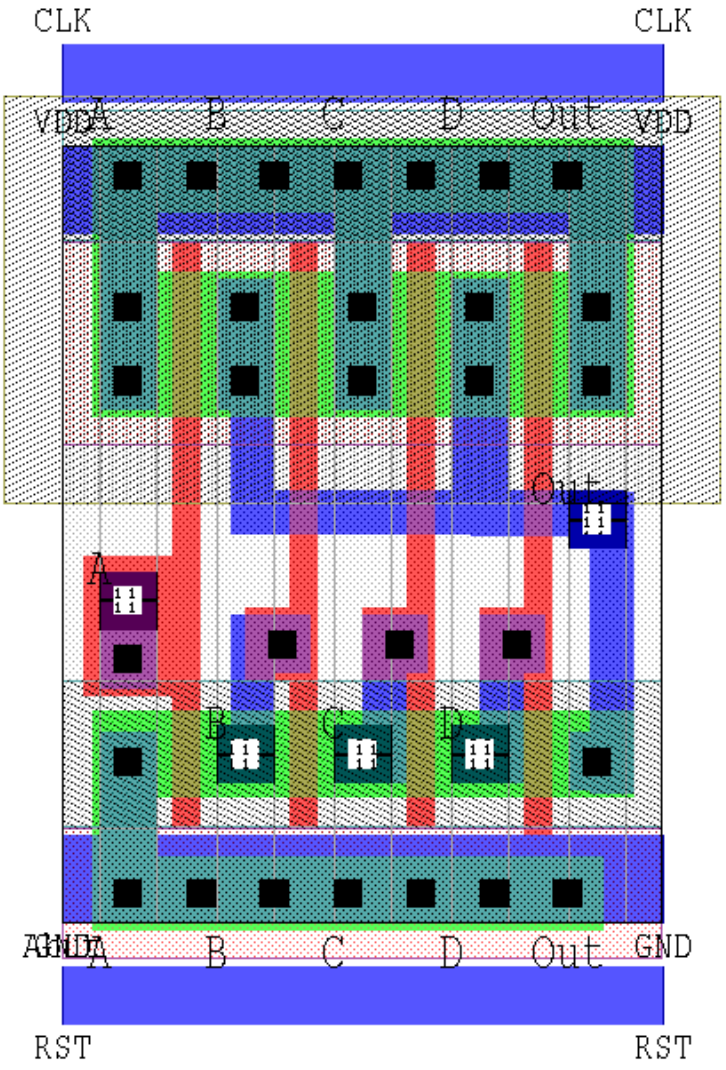
Logic Equation

$$Out = \overline{A \times B \times C \times D}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$Tpd0 \rightarrow 1 \ldots\ldots\ldots 40 + 578 \times C[OUT]$
$Tpd1 \rightarrow 0 \ldots\ldots\ldots 138 + 1850 \times C[OUT]$

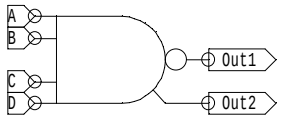


4-Input NAND / AND — NAND4C

Description: 4-Input NAND Gate with Complementary Output

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NAND4C
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NAND4C
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	D	Out1	Out2
0	X	X	X	1	0
X	0	X	X	1	0
X	X	0	X	1	0
X	X	X	0	1	0
1	1	1	1	0	1

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953
D	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	54 λ	2862 λ^2	2.5	1X

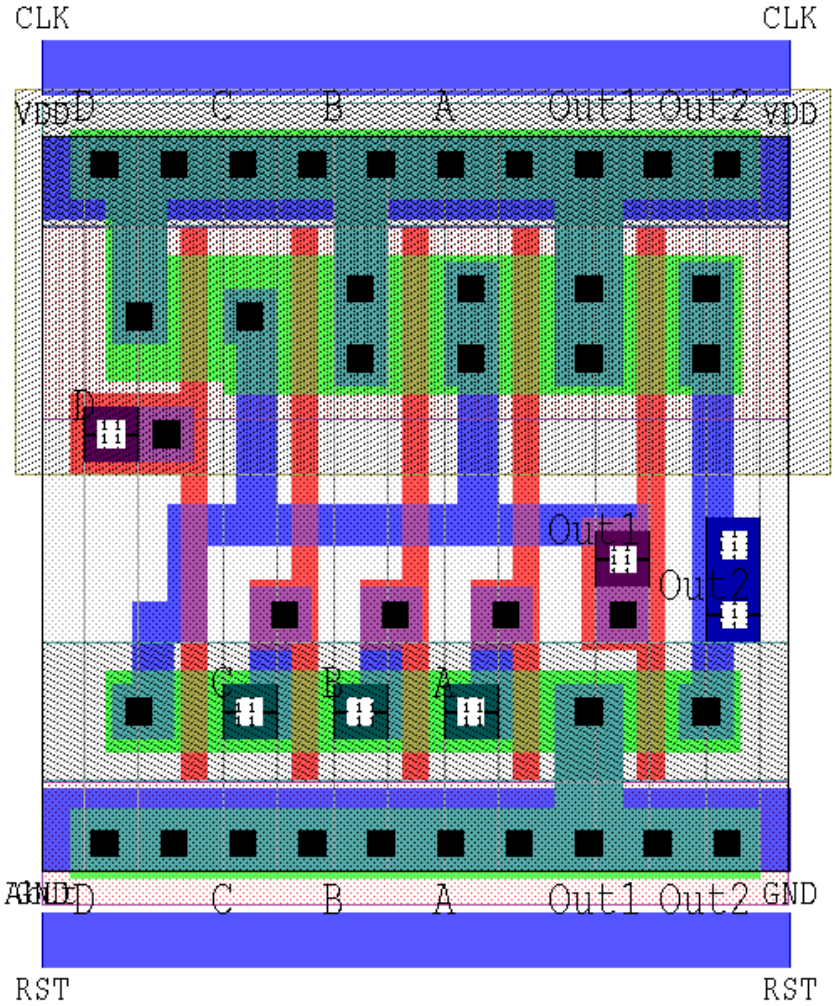
Logic Equation

$Out1 = \overline{A \times B \times C \times D}$
$Out2 = A \times B \times C \times D$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

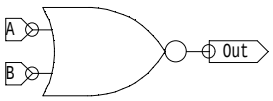
Tpd0 → 1 NAND.....43 + 574 × C[OUT1]
Tpd1 → 0 NAND.....149 + 1848 × C[OUT1]
Tpd0 → 1 AND.....186 + 1848 × C[OUT1] + 1377 × C[OUT2]
Tpd1 → 0 AND.....68 + 574 × C[OUT1] + 940 × C[OUT2]



Description: 2-Input NOR Gate

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NOR2
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NOR2
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out
0	0	1
X	1	0
1	X	0

Capacitance

	Ci(fF)
A	6.953
B	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	25 λ	1325 λ^2	1	1X

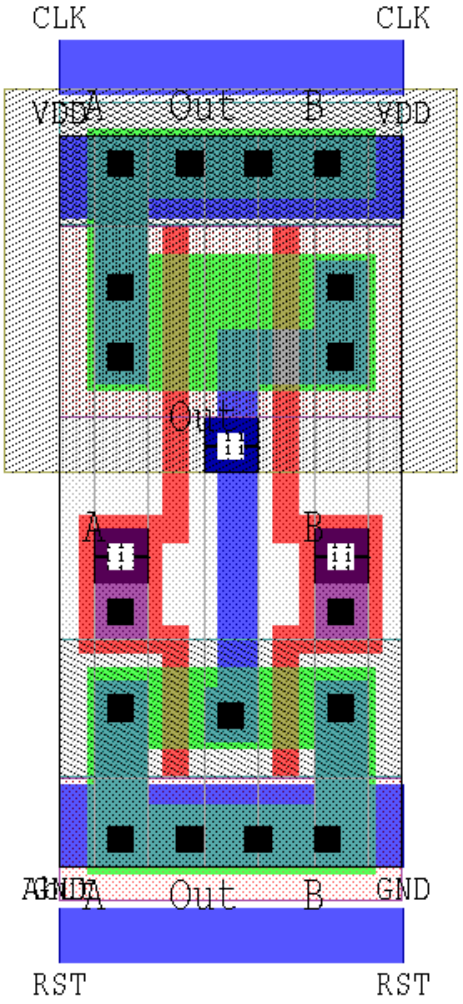
Logic Equation

$$Out = \overline{A + B}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

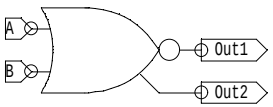
$Tpd0 \rightarrow 1.....31 + 1044 \times C[OUT]$
$Tpd1 \rightarrow 0.....20 + 587 \times C[OUT]$



Description: 2-Input NOR Gate with Complementary Output

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	NOR2C
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	NOR2C
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out1	Out2
0	0	1	0
X	1	0	1
1	X	0	1

Capacitance

	Ci(fF)
A	6.953
B	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	37 λ	1961 λ^2	1.5	1X

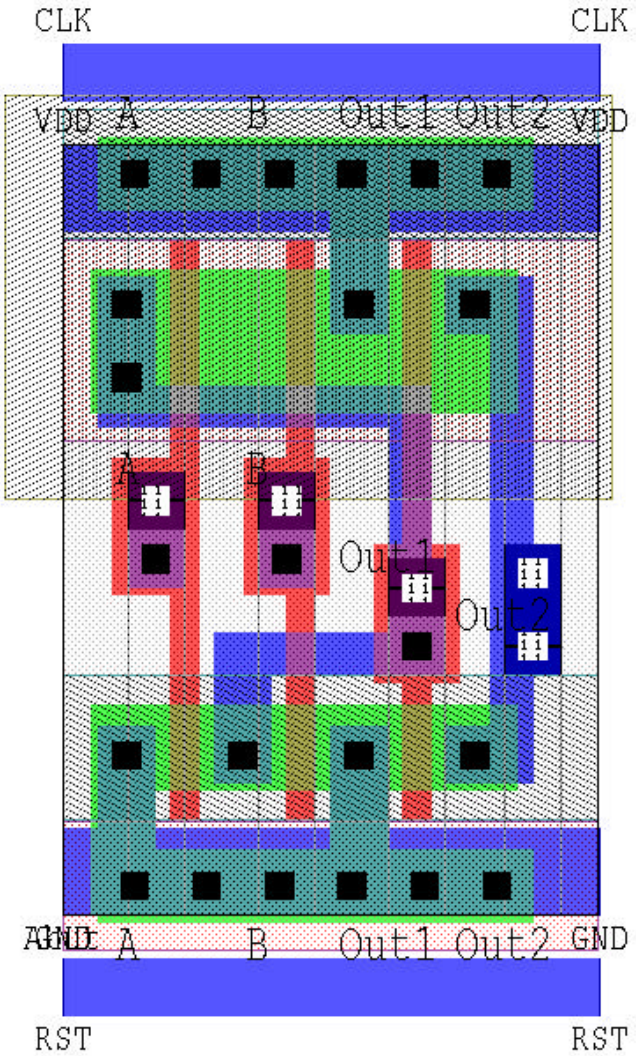
Logic Equation

$Out1 = \overline{A + B}$
$Out2 = A + B$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

Tpd0 → 1 NOR.....37 + 1042 × C[OUT1]
Tpd1 → 0 NOR.....23 + 585 × C[OUT1]
Tpd0 → 1 OR.....42 + 585 × C[OUT1] + 852 × C[OUT2]
Tpd1 → 0 OR.....59 + 1042 × C[OUT1] + 1083 × C[OUT2]

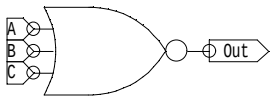


3-Input NOR — NOR3

Description: 3-Input NOR Gate

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	NOR3
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	NOR3
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	Out
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	35 λ	1855 λ^2	1.5	1X

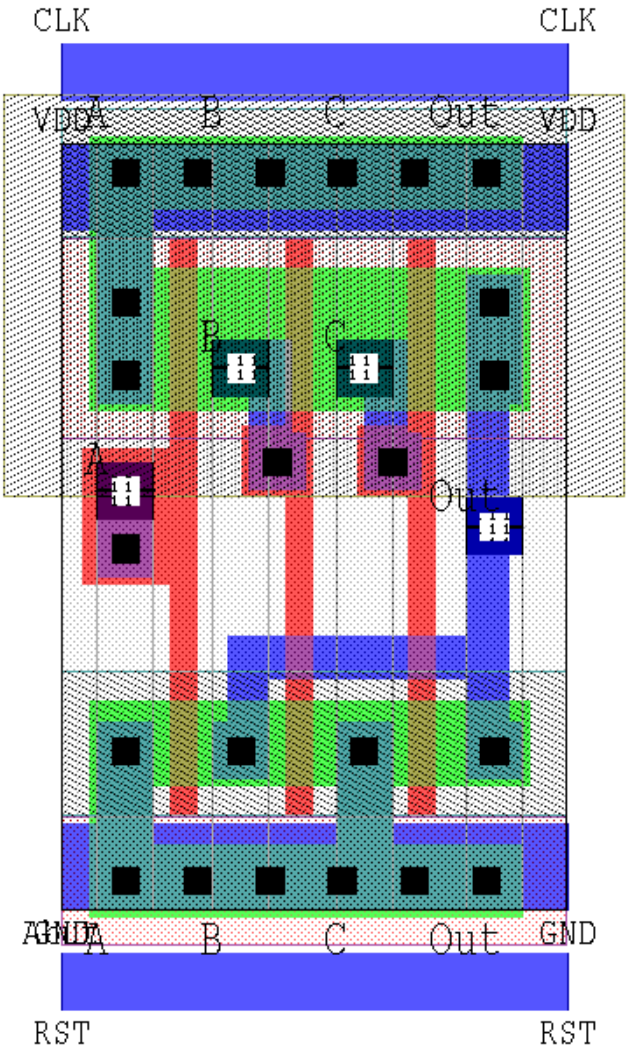
Logic Equation

$$Out = \overline{A + B + C}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$Tpd0 \rightarrow 1 \ldots\ldots\ldots 82 + 1556 \times C[OUT]$
$Tpd1 \rightarrow 0 \ldots\ldots\ldots 31 + 622 \times C[OUT]$

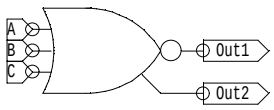


3-Input NOR / OR — NOR3C

Description: 3-Input NOR Gate with Complementary Output

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	NOR3C
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	NOR3C
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	Out1	Out2
0	0	0	1	0
X	X	1	0	1
X	1	X	0	1
1	X	X	0	1

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	45 λ	2385 λ^2	2	1X

Logic Equation

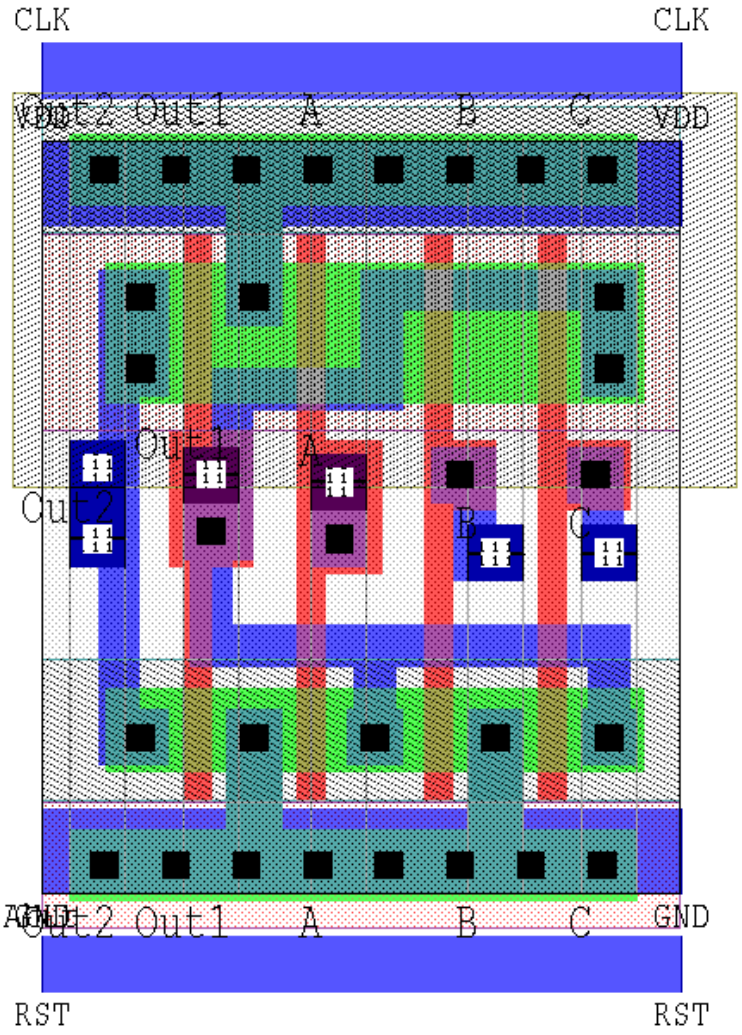
$Out1 = \overline{A + B + C}$

$Out2 = A + B + C$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

Tpd0 → 1 NOR.....89 + 1556 × C[OUT1]
Tpd1 → 0 NOR.....34 + 625 × C[OUT1]
Tpd0 → 1 OR.....57 + 625 × C[OUT1] + 887 × C[OUT2]
Tpd1 → 0 OR.....118 + 1556 × C[OUT1] + 1259 × C[OUT2]

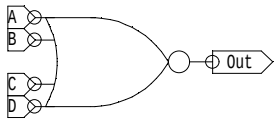


4-Input NOR — NOR4

Description: 4-Input NOR Gate

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NOR4
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NOR4
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	D	Out
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953
D	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	41 λ	2173 λ^2	2	1X

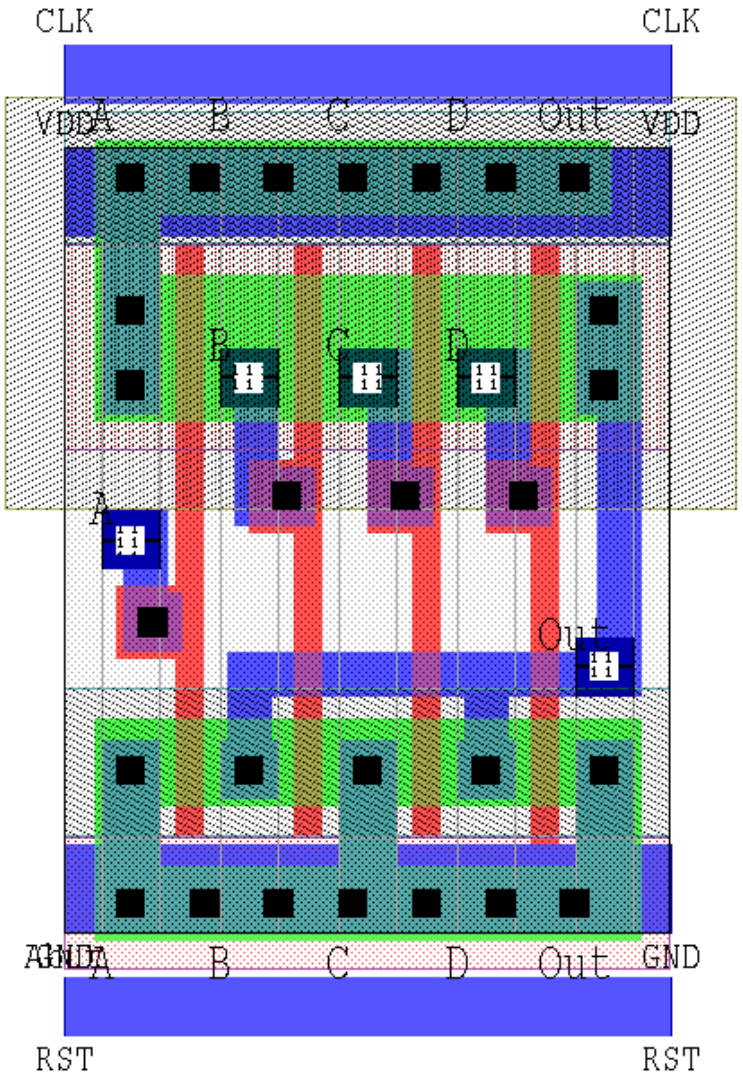
Logic Equation

$$Out = \overline{A + B + C + D}$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

Tpd0 → 1.....131 + 2081 × C[OUT]
Tpd1 → 0..... 33 + 660 × C[OUT]

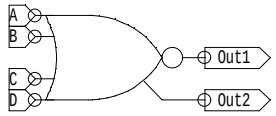


4-Input NOR / OR — NOR4C

Description: 4-Input NOR Gate with Complementary Output

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: NOR4C
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: NOR4C
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	C	D	Out1	Out2
0	0	0	0	1	0
X	X	X	1	0	1
X	X	1	X	0	1
X	1	X	X	0	1
1	X	X	X	0	1

Capacitance

	Ci(fF)
A	6.953
B	6.953
C	6.953
D	6.953

Height	Width	Area	Equivalent Gate	Drive
53 λ	49 λ	2597 λ^2	2.5	1X

Logic Equation

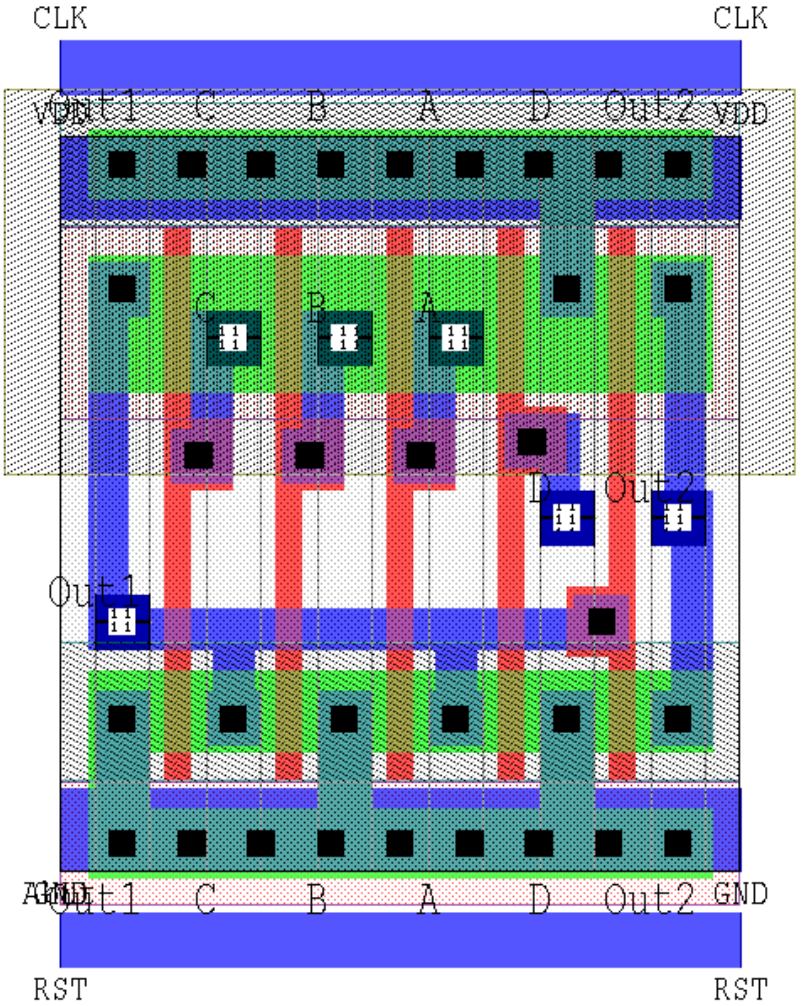
$$Out1 = \overline{A + B + C + D}$$

$$Out2 = A + B + C + D$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

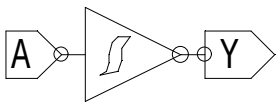
Tpd0→1 NOR.....145 + 2076 × C[OUT1]
Tpd1→0 NOR.....37 + 652 × C[OUT1]
Tpd0→1 OR.....61 + 652 × C[OUT1] + 912 × C[OUT2]
Tpd1→0 OR.....178 + 2076 × C[OUT1] + 1408 × C[OUT2]



Description: Schmitt Trigger Inverter

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: SINV
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: SINV
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance



A	Y
0	1
1	0

	Ci(fF)
A	13.905

Height	Width	Area	Equivalent Gate	Drive
53 λ	53 λ	2809 λ^2	1.5	1X

Logic Equation

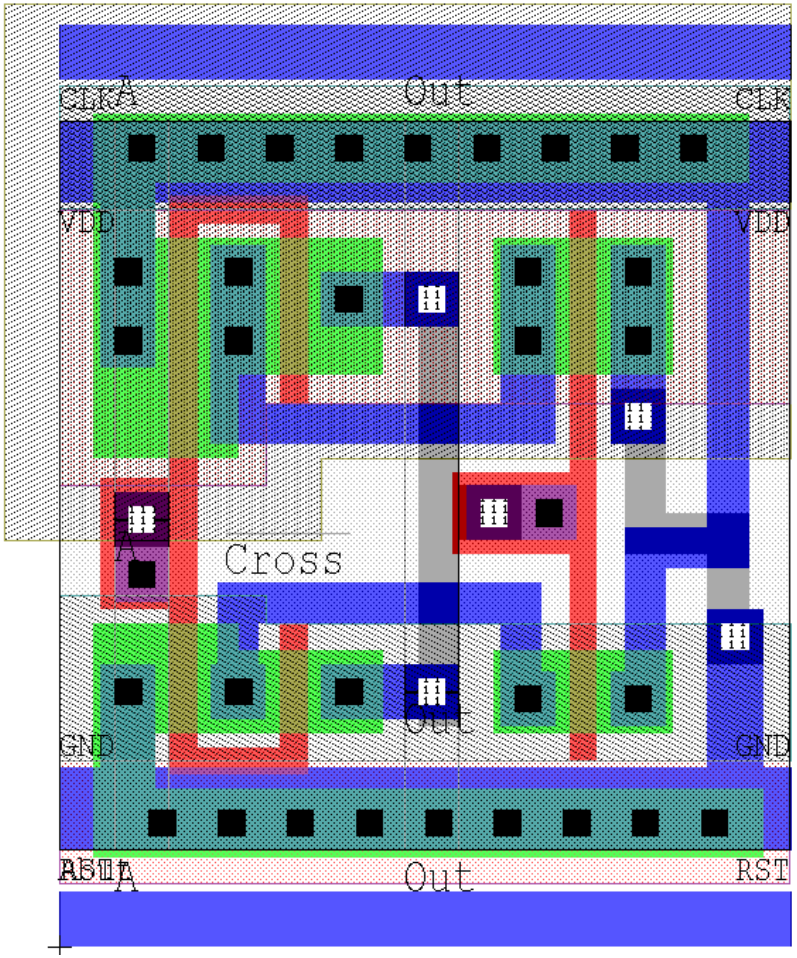
$Out = \overline{A}$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

Tpd0 → 1.....37 + 971 × C[OUT]
Tpd1 → 0.....34 + 983 × C[OUT]

V_{T+} .....1.97V (VDD = 3.3V)
V_{T-} .....1.28V (VDD = 3.3V)

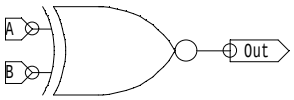


2-Input Exclusive-NOR XNOR2

Description: 2-Input Exclusive-NOR Gate

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	XNOR2
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	XNOR2
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	1

Capacitance

	Ci(fF)
A	13.905
B	13.905

Height	Width	Area	Equivalent Gate	Drive
53 λ	54 λ	2862 λ^2	2.75	1X

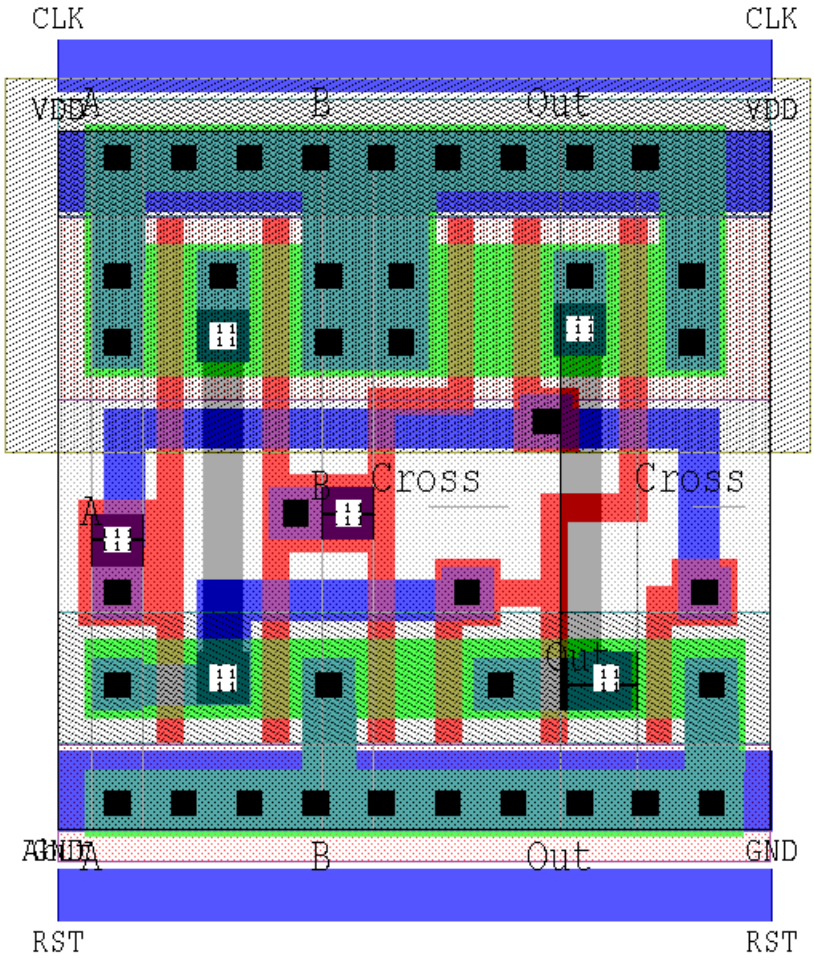
Logic Equation

$$Out = (A \times B) + (\overline{A} \times \overline{B})$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

$Tpd0 \rightarrow 1 \ldots\ldots\ldots 65 + 592 \times C[OUT]$
$Tpd1 \rightarrow 0 \ldots\ldots\ldots 46 + 955 \times C[OUT]$

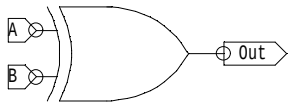


2-Input Exclusive-OR XOR2

Description: 2-Input Exclusive-OR Gate

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	XOR2
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	XOR2
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol



Truth Table

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

Capacitance

	Ci(fF)
A	13.905
B	13.905

Height	Width	Area	Equivalent Gate	Drive
53 λ	54 λ	2862 λ^2	2.75	1X

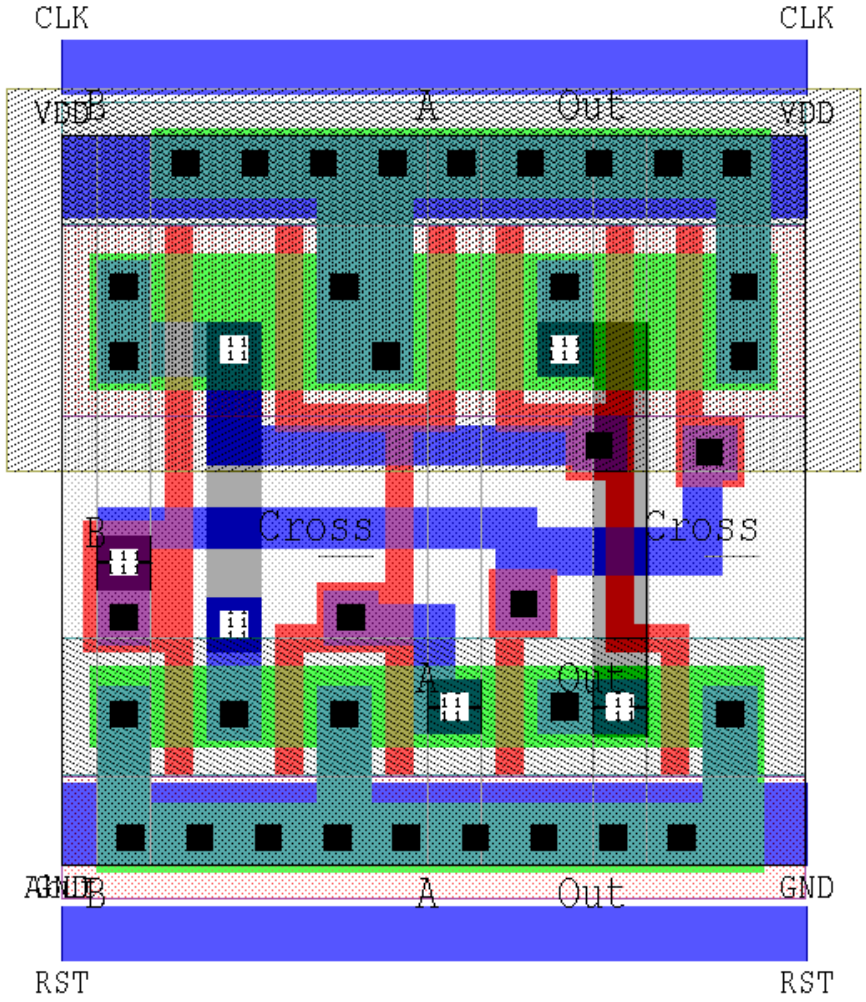
Logic Equation

$$Out = (A \times \overline{B}) + (\overline{A} \times B)$$

Delay Characteristics:

$$T_{pd} = t_0 + \frac{dt}{dc} \times C_L$$

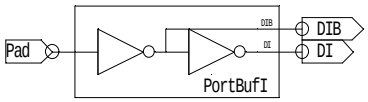
$Tpd0 \rightarrow 1.....48 + 991 \times C[OUT]$
$Tpd1 \rightarrow 0.....64 + 634 \times C[OUT]$



Description: Buffered Input Port with Complementary Signals

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells
Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: PortBufI
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: PortBufI
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance



PAD	DI	DIB
0	0	1
1	1	0

N/A

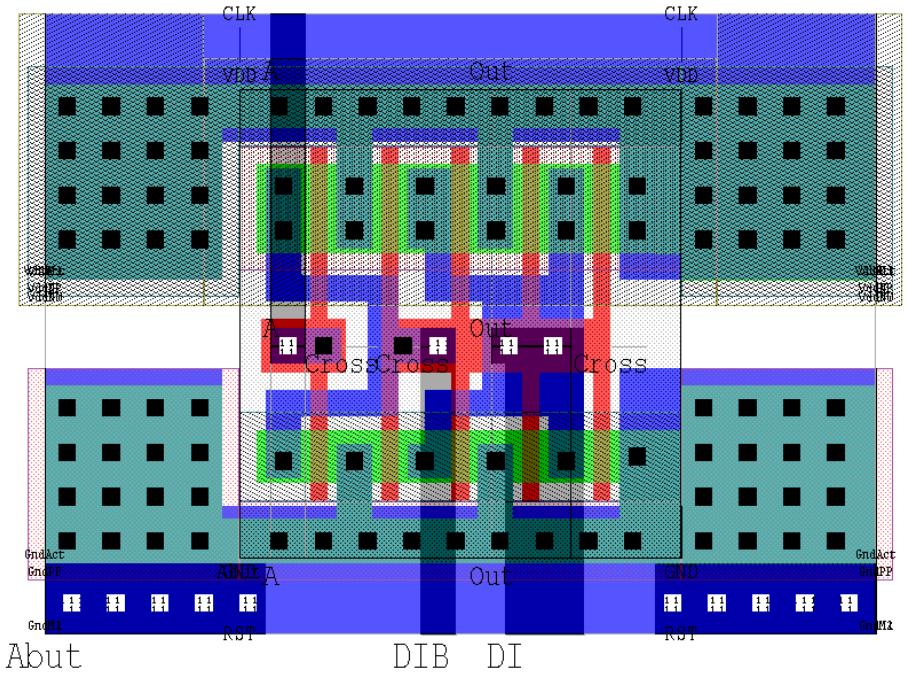
Height	Width	Area	Equivalent Gate	Drive
70 λ	94 λ	6580 λ^2	N/A	N/A

Logic Equation

$DI = In$

$DIB = \overline{In}$

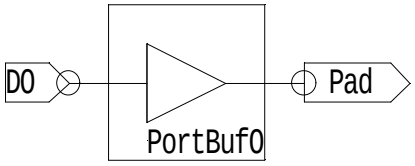
Delay Characteristics: N/A



Output Port — PORTBUFO

Description: Buffered Output Port used for Core routing

Library: Tanner mAMIs05DL
Primitive Set: Tanner SCMOS.Cells, Tanner.TIB.Samples
Schematic: S-Edit
File: TannerLb\scmos\scmos.sdb
Module: PortBufO
Mask layout: L-Edit
File: TannerLb\scmos\scmos.tdb
Cell: PortBufO
Mapping Macros: GateSim: TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR: TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
		N/A

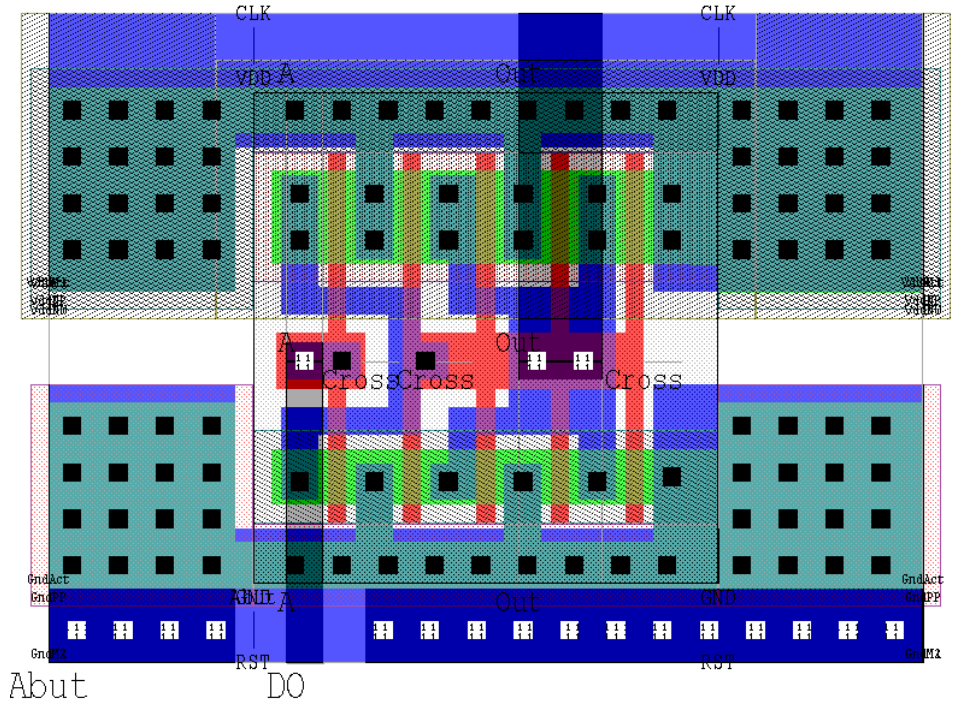
DO	PAD
0	0
1	1

Height	Width	Area	Equivalent Gate	Drive
70 λ	94 λ	6580 λ^2	N/A	N/A

Logic Equation

DO = Out

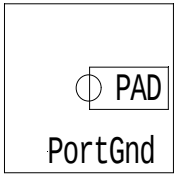
Delay Characteristics: N/A



Ground Port PORTGND

Description: Ground Port used for core routing

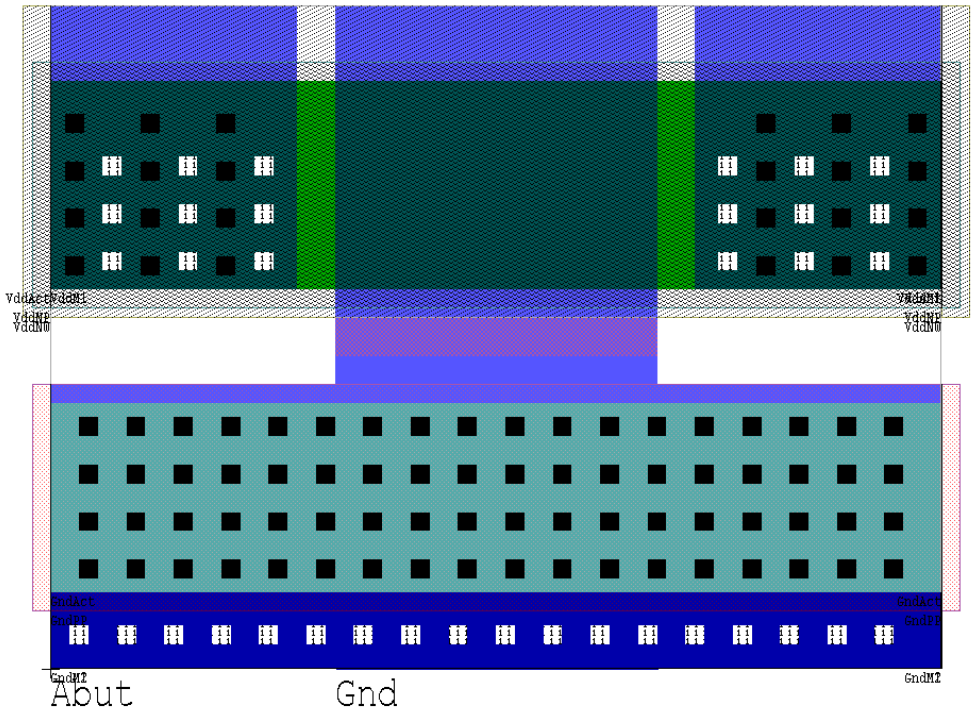
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	PortGnd
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	PortGnd
Mapping Macros: GateSim:	TannerLb\nettran\scmos\scms2sim.mac	
L-Edit/SPR:	TannerLb\nettran\scmos\scms2tpr.mac	

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
70 λ	94 λ	6580 λ^2	N/A	N/A

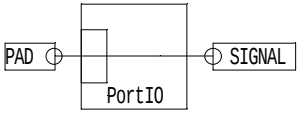
Logic Equation
Port = 0

Delay Characteristics: N/A



Description: Input/Output Port

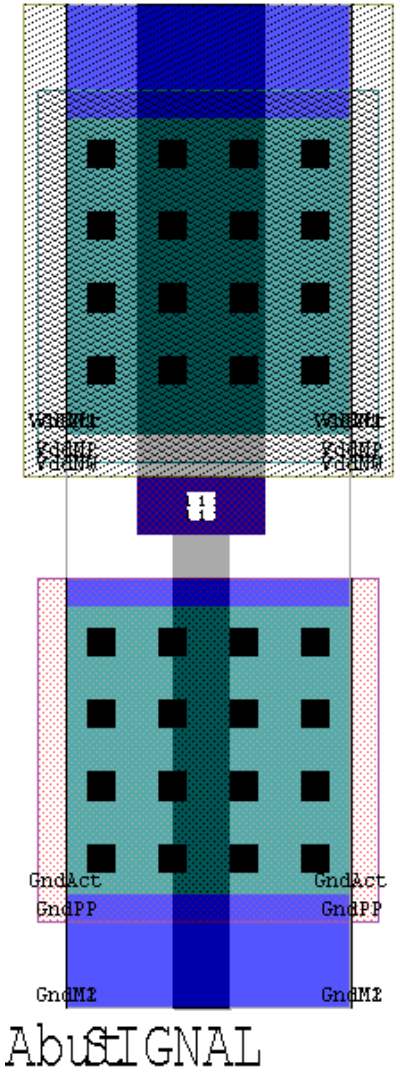
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	PortIO
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	PortIO
Mapping Macros: GateSim:		TannerLb\nettran\scmos\scms2sim.mac
L-Edit/SPR:		TannerLb\nettran\scmos\scms2tpr.mac

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
70 λ	20 λ	1400 λ^2	N/A	N/A

Logic Equation

Delay Characteristics: N/A



Description: Ring Corner Port

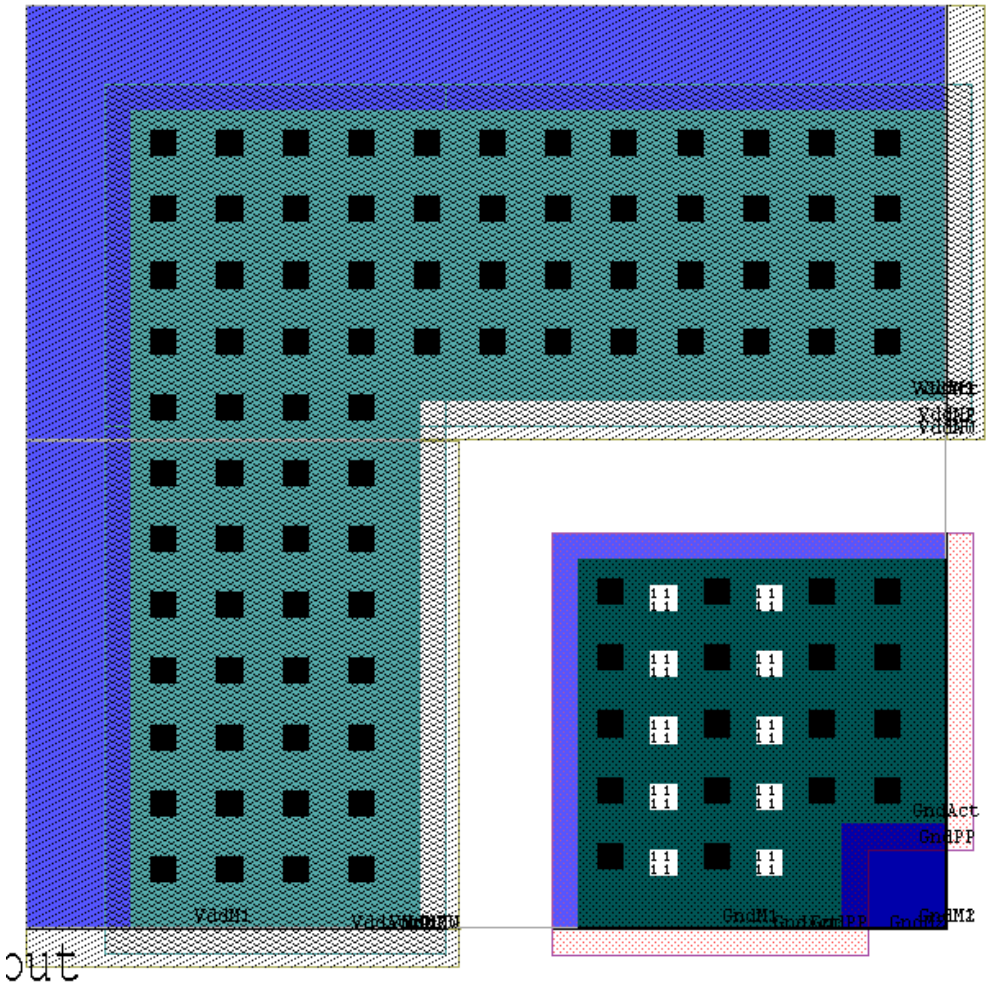
Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	PortRC
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	PortRC
Mapping Macros: GateSim:	TannerLb\nettran\scmos\scms2sim.mac	
L-Edit/SPR:	TannerLb\nettran\scmos\scms2tpr.mac	

Logic Symbol	Truth Table	Capacitance
N/A	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
70 λ	70 λ	4900 λ^2	N/A	N/A

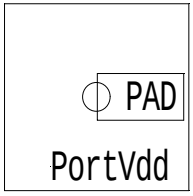
Logic Equation
N/A

Delay Characteristics: N/A



Description: Power Port used for core routing

Library: Tanner mAMIs05DL	Primitive Set:	Tanner SCMOS.Cells Tanner.TIB.Samples
Schematic: S-Edit	File:	TannerLb\scmos\scmos.sdb
	Module:	PortVdd
Mask layout: L-Edit	File:	TannerLb\scmos\scmos.tdb
	Cell:	PortVdd
Mapping Macros: GateSim:	TannerLb\nettran\scmos\scms2sim.mac	
L-Edit/SPR:	TannerLb\nettran\scmos\scms2tpr.mac	

Logic Symbol	Truth Table	Capacitance
	N/A	N/A

Height	Width	Area	Equivalent Gate	Drive
70 λ	94 λ	6580 λ^2	N/A	N/A

Logic Equation
$Port = 1$

Delay Characteristics: N/A