## The University of Alabama in Huntsville Electrical and Computer Engineering Department CPE 221 01 Test 1 September 27, 2018

## This test is closed book, closed notes. You may not use a calculator. You should have the 6 page ARM Instruction Reference. <u>You must show your work to receive full credit.</u>

		Name:
1.	(1 point) A consists of 8 bits.	
2.	(1 point) A	logic element is a circuit whose output depends
	only on its current inputs.	
3.	(1 point) An AND gate has a controlling value	e of
4.	(1 point) The symbol for an inverter is	
5.	(1 point) The ARM processor has re	gisters.

6. (10 points) Convert decimal +327 and +-456 to binary, using the signed-2's complement representation and enough digits to accommodate the numbers.

7. (3 points) What is the decimal equivalent of  $11001100_5$  (assume positional notation and unsigned integer formats)?

- 8. (12 points) If  $r1 = 0 \times 000F$  0FFF and r2 = 4, what is the value of r0 after each of the following instructions has been executed? Assume that each instruction uses the same data.
  - (a) ADD r0, r1, r1, LSL #9

(b) ADD r0, r1, r1, ROR #5

(c) ADD r0, r1, r1, LSR r2

- 9. (10 points) For each of the following operations on 6 bit signed numbers, calculate the values of the C, Z, V, and N flags
  - (a) 101111 + 001101 (b) 110011 + 001001

10.

1.	Explain the effect of each of the following instructions using register transfer notation.						
2.	. Give the value in $r2$ after each instruction executes.						
3.	Give the value of the effective address.						
Assume that $r2$ contains the initial value $0 \times FF001110$ and that $r0$ contains $0 \times FFFF$ 87 Use these initial values for each instruction individually.							
(a)	LDR r1, [r2]						

(15 points) For each of the following cases,

Register Transfer	
r2	
Effective Address	
(b) STR r1, [r2,	#2_1101]
Register Transfer	
r2	
- Effective Address	
-	
(c) LDR r1, [r2,	#0x2C]!
Register Transfer	
r2	
Effective Address	
-	
(d) STR r1, [r2],	# – 4
(4) 511( 11) [12])	11 1
Register Transfer _	
r2 _	
Effective Address	
(e) LDR r1, [r2, 1	20, ASR #3]
Register Transfer r2	
Effective Address	

11. (25 points) Consider the following ARM program. Trace the values of the registers shown as they change during program execution. Also, trace the writes to memory by the STR instructions. There may be unused columns or rows in the tables. If you need to add columns or rows, you may do so. DCD 1 reserves one word of storage and sets it equal to 1. SPACE 3 reserves 3 bytes of memory but does not give those bytes a value.

		AREA	PROB 11, CODE, READONLY
		ENTRY	
0		ADR	r0, x
4		ADR	
8		ADR	
12			r3, size
16		LDR	
	1000		
	тоор	CMP	
24		BGE	
28			r5, [r0], #4
32			r6, [r1], #4
36		CMP	r5, r6
40		STRGT	r5, [r2], #4
44		STRLE	r6, [r2], #4
48		ADD	r4, r4, #1
52		В	loop
56	done	В	done
			100, 3, -1, 2, 4, 4
			-53, 247, 95, -7, 481, 91
108	-	SPACE	
132		DCD	
	size		6
100	SILE	END	0
		ыND	

r0									
r1									
r2									
r3									
r4									
r5									
r6									

Results of the  ${\tt STR}$  instruction.

Contents

12. (20 points) Complete the ARM assembly language program below so that it implements the following C++ statements.

int size = 10; for i = 0; i < size; i++) ndigit[i] = i + 1; AREA PROB\_12, CODE, READONLY ENTRY LDR r0, i LDR r1, size

ndigit	SPACE	40
i	DCD	0
size	DCD	10
	END	