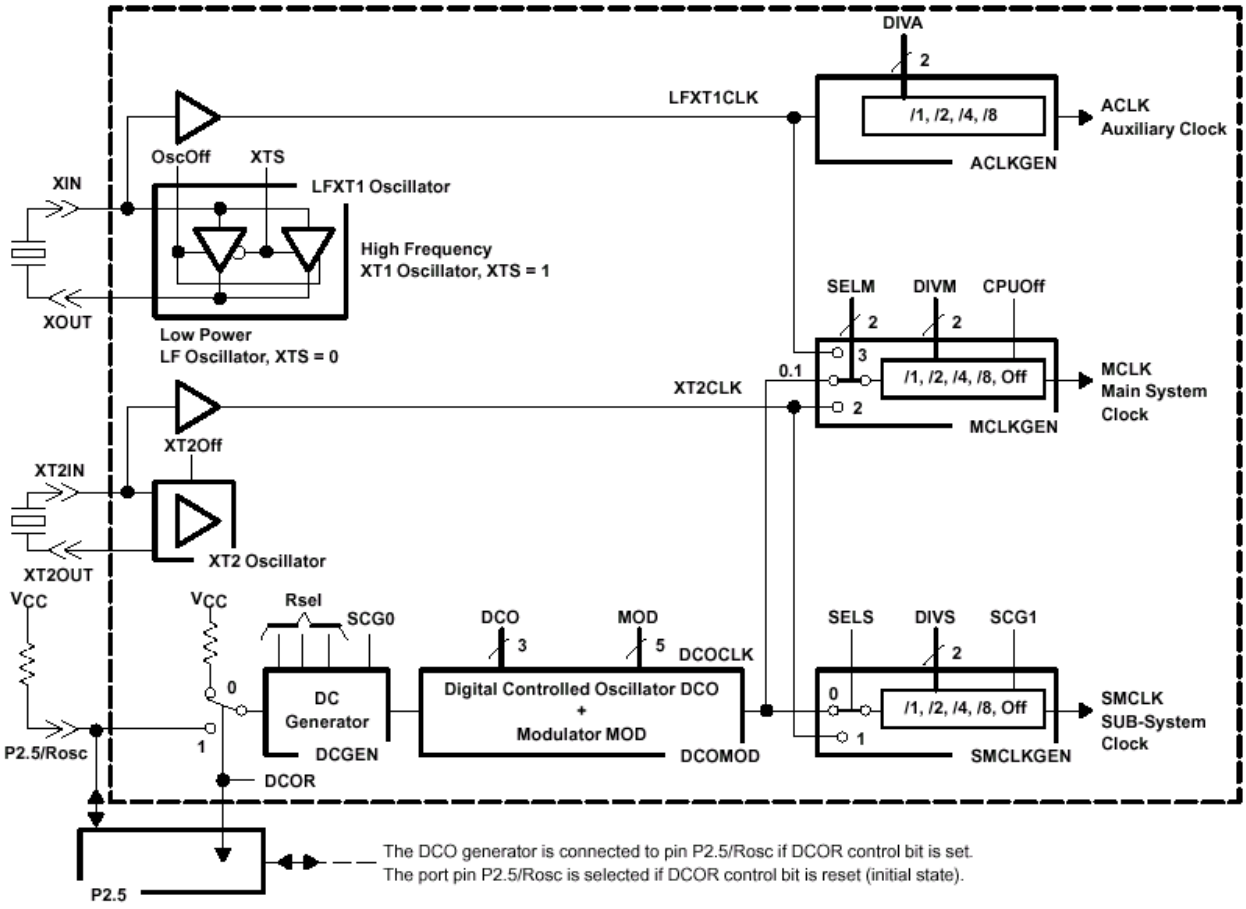
The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE/EE 421/521 01
Homework #1 Solution
Fall 2004

1. (30 points) Microcontroller system is using 8MHz crystal connected to XIN input and 3V power supply.



PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	

BCSCTL1:	XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel2	Rsel1	Rsel0
BCSCTL2:	SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
DCOCTL:	DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0

Set the following modes of operation:

a) (15 points) DC generated MCLK to 750 KHz, SMCLK to 93.75 KHz.

BCSCTL1: 0x___=	1	0	0	0	0	0	1	1
	XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel2	Rsel1	Rsel0
BCSCTL2: 0x___=	0	0	0	0	0	1	0	0
	SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
DCOCTL: 0x___=	0	1	1	0	0	0	0	0
	DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0

b) (15 points) processor clock to 8MHz, ACLK to 4MHz.

BCSCTL1: 0x___=	1	1	1	0	0	0	0	0
	XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel2	Rsel1	Rsel0
BCSCTL2: 0x___=	1	1	0	1	0	0	0	0
	SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
DCOCTL: 0x___=	0	0	0	0	0	0	0	0
	DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0

NOTE:

- XT5V bit should be 0.
- DCOR: use internal Rosc
- For all DIV fields:

DIV field value	0	1	2	3
Divided by:	1	2	4	8

2. (15 points)

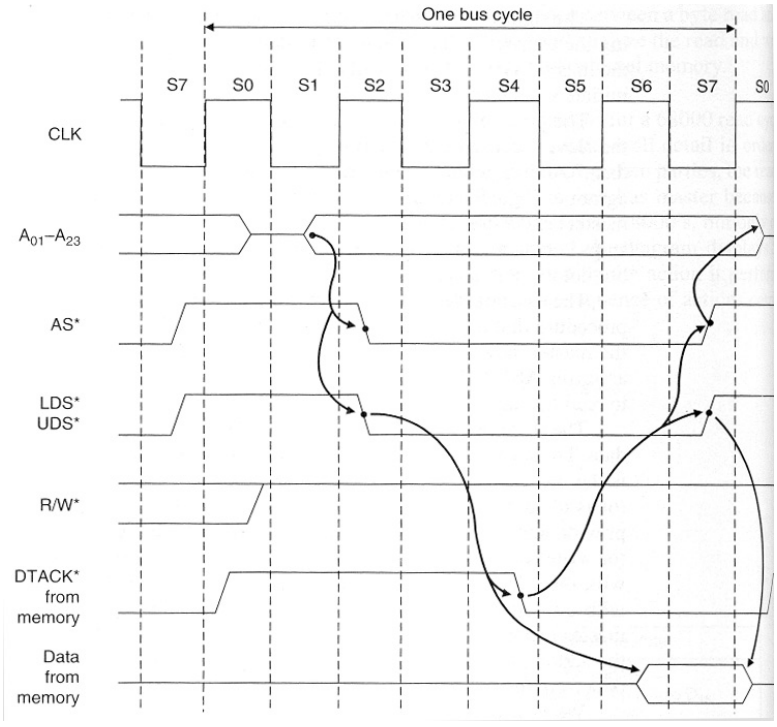
a) (5 points) What is the state (**H**igh/**L**ow) of 68K signal lines for the following operations?

Solution:

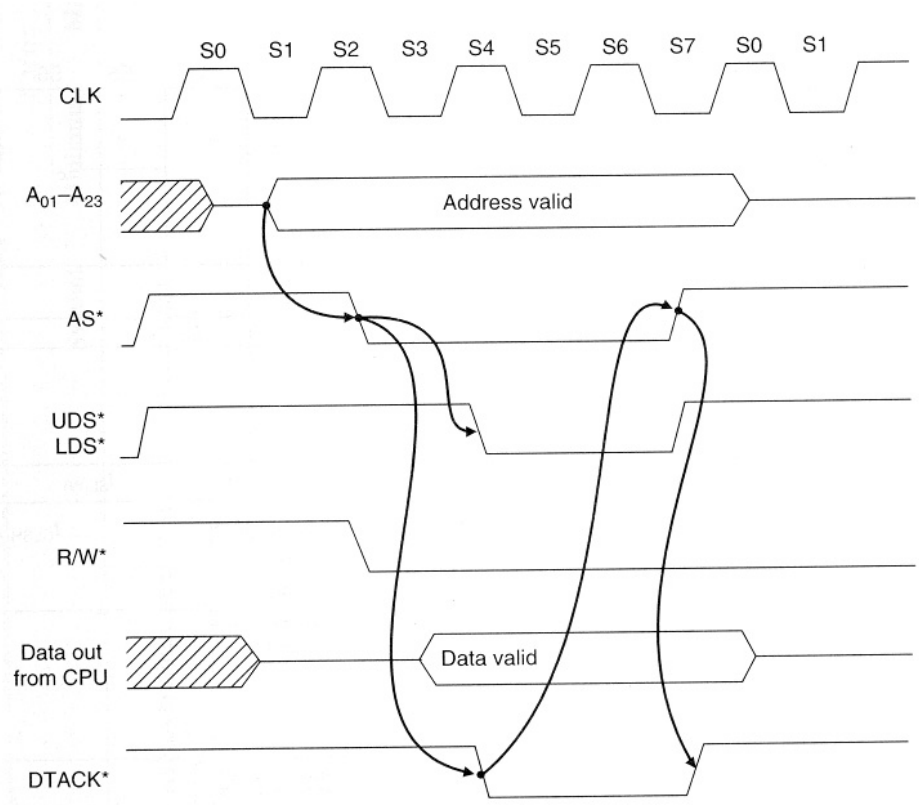
Operation	Word read	Byte read, Even address	Byte write, Odd address
AS*	L	L	L
R/W*	H	H	L
UDS*	L	L	H
LDS*	L	H	L

b) (5 points) Describe the 68000's read cycle explaining the actions that take place and the relationship between them. Give the simplified timing diagram.

State S0	R/W*output is set high to terminate any previous write cycle.
State S1	The 68000 puts the address on the address bus. It remains valid for the duration of the read cycle.
State S2	The 68000 asserts AS* and LDS*/UDS* to indicate that the address is valid.
State S3	No signals change state.
State S4	DTACK* must go low before the end of S4, if wait states are not required.
State S5	No signals change state.
State S6	Data from the memory is latched by the 68000 at the end of S6 state.
State S7	The address and data strobes are de-asserted to terminate the read cycle.



c) (5 points) Describe the 68000's write cycle explaining the actions that take place and the relationship between them. Give the simplified timing diagram.



3. (55 points) Design a microcomputer system with a MC68000 microprocessor that features
1) 256KB of supervisor program memory residing at the address $04000 using 32K×8 EPROMs modules
2) 64KB of supervisor data memory using 4K×8bit static RAM modules, and
3) 128KB of user program and data memory using 32K×8bit static RAM modules.
All three memories reside in consecutive address windows. Design necessary logic to generate:

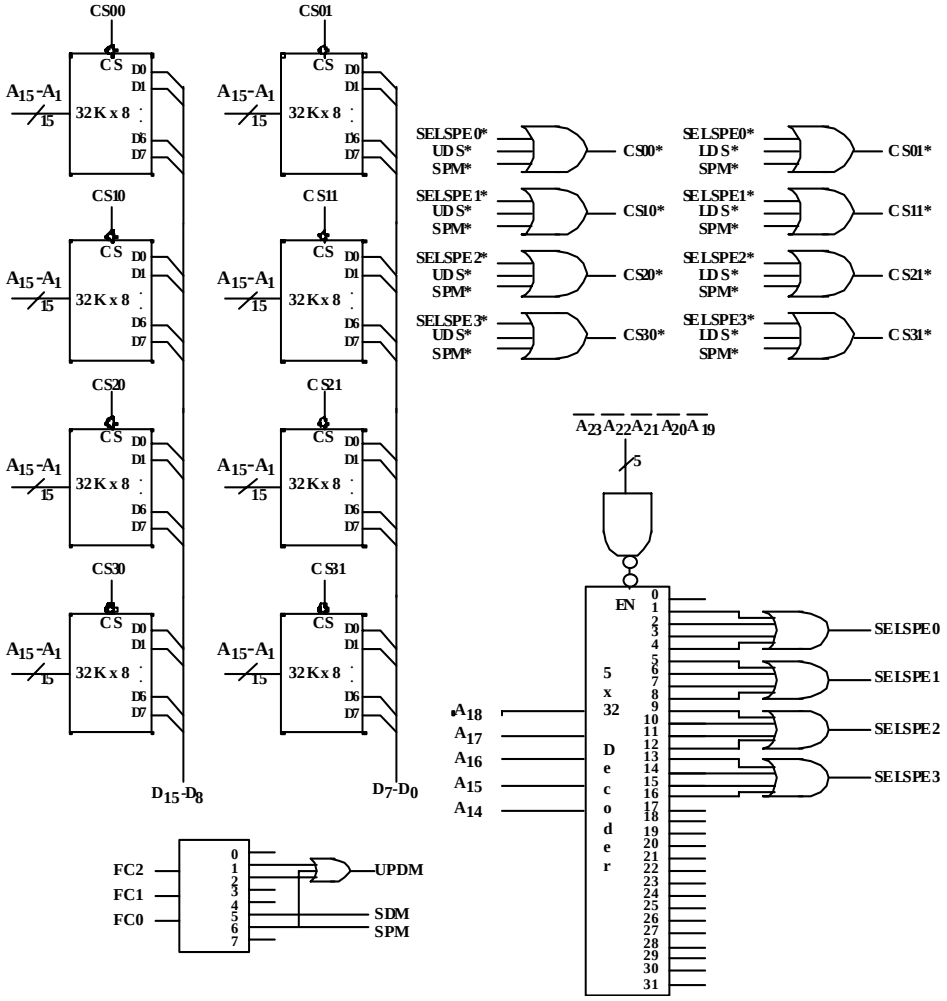
- Address decoding signals (CS*)
- Control signals (WE*, OE*)

Tie all OE* low. OR the CS and the R/W* to generate WE* for each chip.

The memory map follows:

SPM	00 4000	0000 0000 0100 0000 0000 0000
	+3 FFFF	
	04 3FFF	0000 0100 0011 1111 1111 1111
SDM	04 4000	0000 0100 0100 0000 0000 0000
	+0 FFFF	
	05 3FFF	0000 0101 0011 1111 1111 1111
UPDM	05 4000	0000 0101 0100 0000 0000 0000
	+1 FFFF	
	06 3FFF	0000 0110 0011 1111 1111 1111

The address decoding for the supervisor program memory is as follows:



The address decoding for the user program and data memory is as follows
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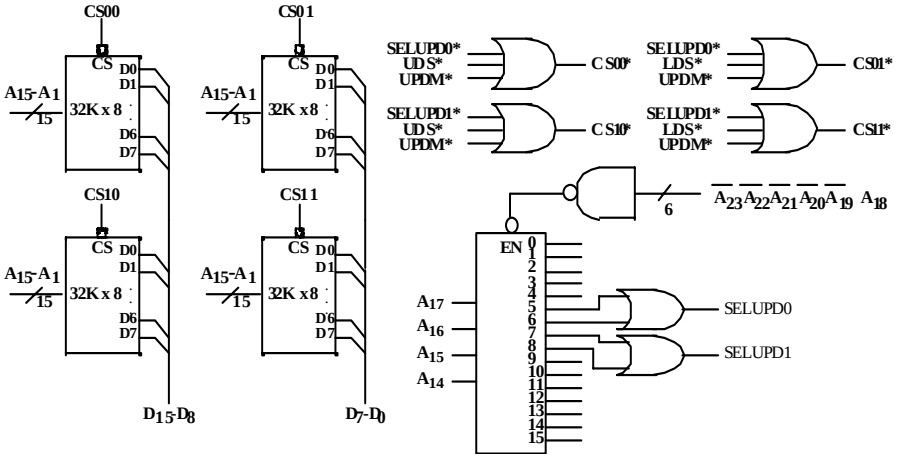

The address decoding for the supervisor data memory is as follows: