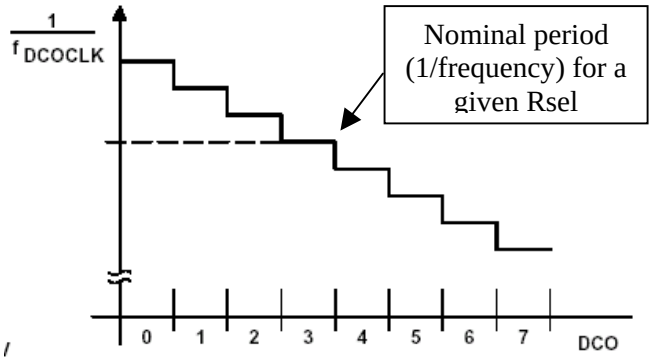
The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE/EE 421/521 01
Test 2
December 1, 2004

Name: _____

1. (30 points) A MSP430 microcontroller system is using a 32KHz crystal connected to the LFXT1 Oscillator, an 8MHz crystal connected to the XT2 Oscillator, and a 3V power supply. See **Appendix (pages 6-9)** for necessary information.

Datasheet specifications:

$f_{Rsel+1} / f_{Rsel} = 1.65$,
$f_{DCO+1} / f_{DCO} = 1.12$,
DCOR: use internal R_{osc}



Set the following modes of operation (If the bit can be either 0 or 1, put d):

a) (10 points) processor clock (MCLK) to 2 MHz, ACLK to 16 KHz, SMCLK to 180 KHz.

BCSCTL1:								
	XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel2	Rsel1	Rsel0
BCSCTL2:								
	SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
DCOCTL:								
	DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0

b) (10 points) processor clock to 590 KHz, SMCLK to 295 KHz, and ACLK to 4 KHz.

BCSCTL1:								
	XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel2	Rsel1	Rsel0
BCSCTL2:								
	SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
DCOCTL:								
	DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0

c) (10 points) What should be the value of MOD if MCLK needs to be set to **2.6 MHz** for the system that doesn't use external oscillators (uses only DCO)? Give values for Rsel, DCO, and MOD. Show how you came up with the result. [*Hint*: use the formula $T=((32-MOD)*T_{DCO} + MOD*T_{DCO+1})/32$]

2. (45 points) Using given memory components, design a memory subsystem for an MC68000-based microcomputer system with the following characteristics:

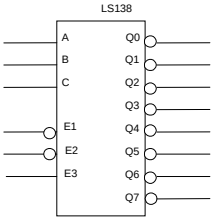
a. 128 KB of supervisor program memory (EPROM) residing at address $00 0000
b. 128 KB of supervisor data memory (out of 16K RAM) residing in the consecutive address window, and
c. 64 KB of user program/data memory (out of 32K RAM) beginning at the address $08 0000.

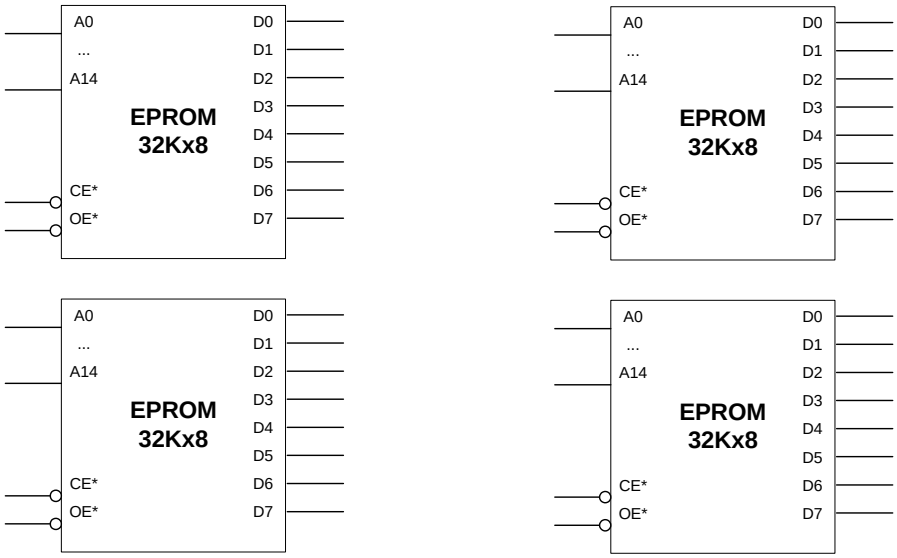
Use LS138 decoder(s) (3 to 8) plus any other logic gates for address decoding, and generate:

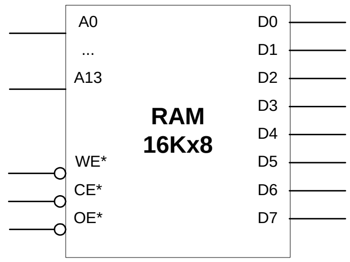
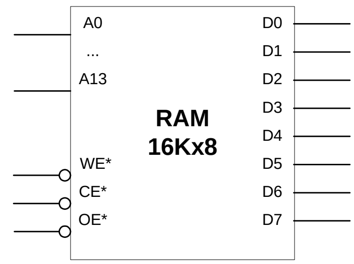
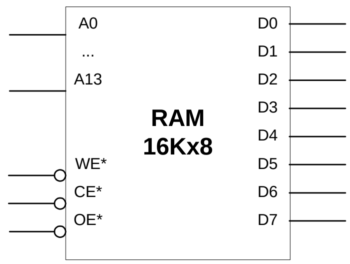
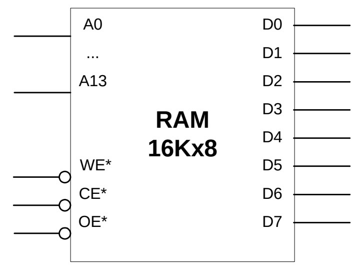
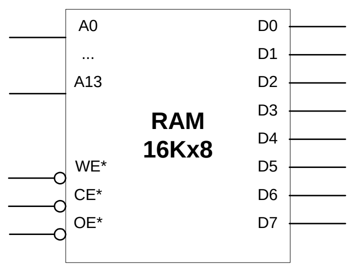
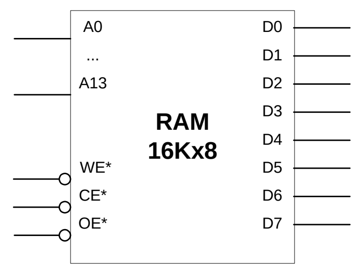
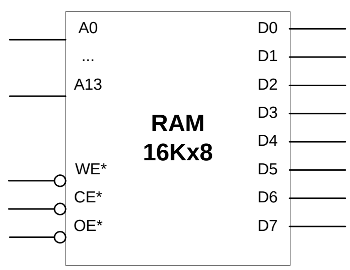
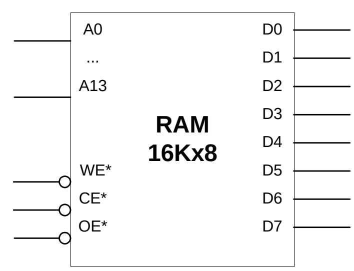
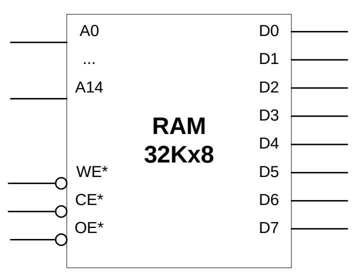
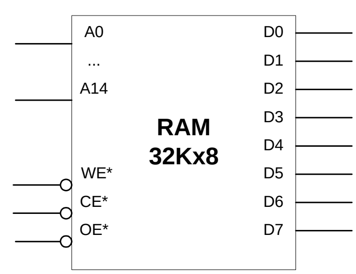
- Address decoding signals (CS*)
- Control signals (WE*, OE*)

Use FC0-FC2 signals to make sure that memory is properly accessed. Make sure that the 68000 has access to user program and data space in supervisor mode.

Function Code Output			Processor Cycle Type
FC2	FC1	FC0	
0	0	0	Undefined, reserved
0	0	1	User data
0	1	0	User program
0	1	1	Undefined, reserved
1	0	0	Undefined, reserved
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	CPU space (interrupt acknowledge)






A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A13
WE*
CE*
OE*
RAM
16Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A14
WE*
CE*
OE*
RAM
32Kx8
D0
D1
D2
D3
D4
D5
D6
D7

A0
...
A14
WE*
CE*
OE*
RAM
32Kx8
D0
D1
D2
D3
D4
D5
D6
D7

3. (20 points) A microcontroller system operates with a system frequency of 200 Hz (repeat the following sequence: a/d conversion, process data, real-time clock, idle). What is the expected system operation time if the system is supplied with 720mAh capacity battery? The power consumption of different components is:

- Analog interface circuit 1 mA, cycle operation time - 300 μs.
- Microcontroller in active mode 420 μA, cycle processing time:
- 50 μs with probability 25%
- 75 μs with probability 50%
- 140 μs with probability 25%
- Microcontroller in idle mode 1.8 μA.
- Real Time Clock 300 μA, cycle operation time - 90 μs.
- LCD display 20 μA, always active.

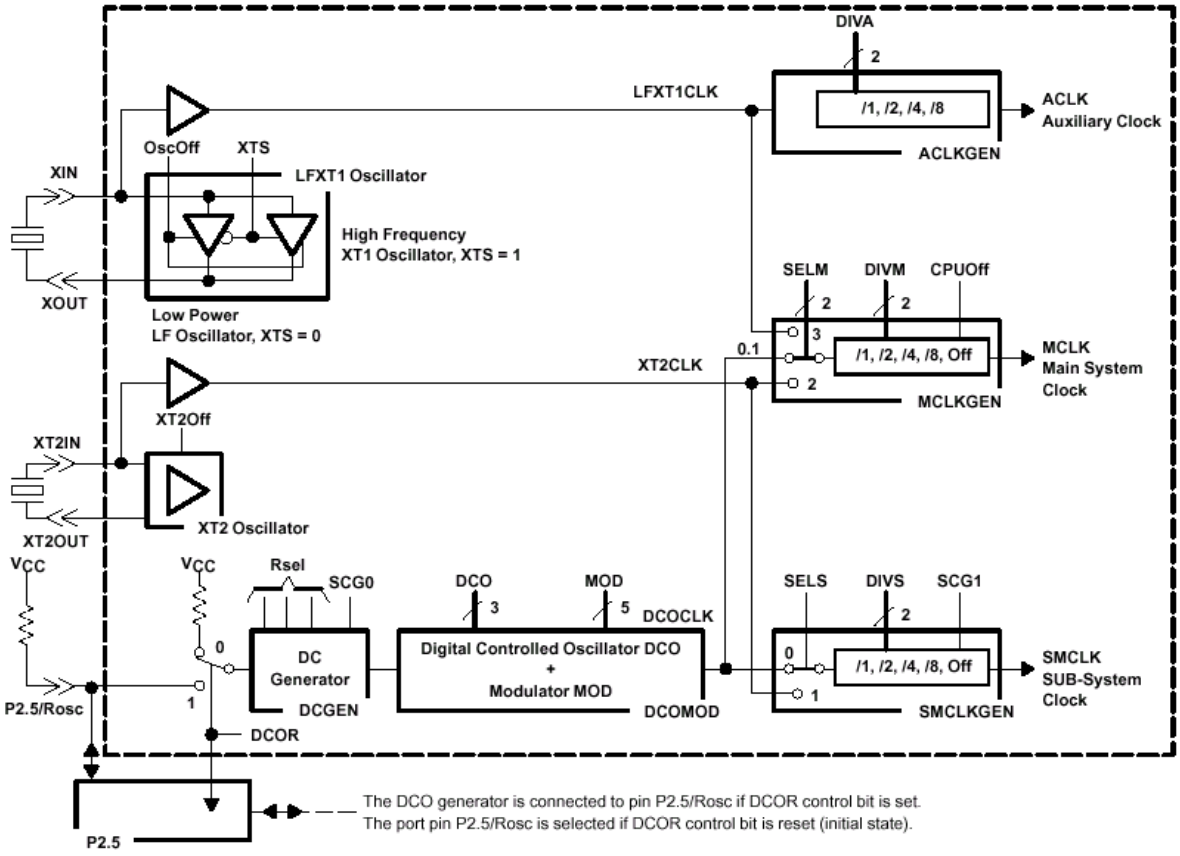
4. (1 point) The ability to use different addressing modes for both source and destination is referred to as instruction _____.

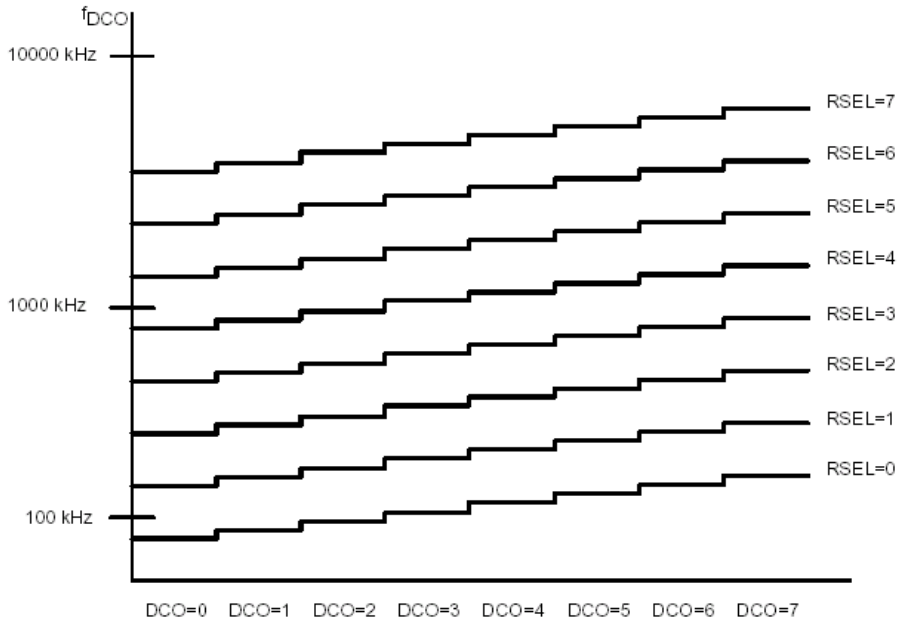
5. (2 points) The MSP430 supports _____addressing modes for source operands and _____ addressing modes for destination operands..

6. (2 points) _____ and _____ are two addressing modes used in the MSP430.

Appendix

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	f_{DCO40} × 1.7	f_{DCO40} × 2.1	f_{DCO40} × 2.5	MHz
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$S_{(Rsel)}$	$S_R = f_{Rsel+1} / f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1} / f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 30)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 30)	V_{CC} = 2.2 V/3 V	0	5	10	%/V





7.5 Basic Clock Module Control Registers

The Basic Clock Module is configured using control registers DCOCTL, BCSCTL1, and BCSCTL2, and four bits from the CPU status register: SCG1, SCG0, OscOff, and CPUOFF. User software can modify these control registers from their default condition at any time. The Basic Clock Module control registers are located in the byte-wide peripheral map and should be accessed with byte (.B) instructions.

Register	Short Form	Register Type	Address	Initial State
DCO control register	DCOCTL	Read/write	056h	060h
Basic clock system control 1	BCSCTL1	Read/write	057h	084h
Basic clock system control 1	BCSCTL2	Read/write	058h	reset

7.5.1 Digitally-Controlled Oscillator (DCO) Clock-Frequency Control

DCOCTL is loaded with a value of 060h with a valid PUC condition.

DCOCTL 056h

7							0
DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0
rw–0	rw–1	rw–1	rw–0	rw–0	rw–0	rw–0	rw–0

MOD.0 .. MOD.4: The MOD constant defines how often the discrete frequency f_{DCO+1} is used within a period of 32 DCOCLK cycles. During the remaining clock cycles (32–MOD) the discrete frequency f_{DCO} is used. When the DCO constant is set to seven, no modulation is possible since the highest feasible frequency has then been selected.

DCO.0 .. DCO.2: The DCO constant defines which one of the eight discrete frequencies is selected. The frequency is defined by the current injected into the dc generator.

7.5.2 Oscillator and Clock Control Register

BCSCTL1 is affected by a valid PUC or POR condition.

BCSCTL1 057h

7							0
XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel.2	Rsel.1	Rsel.0
rw–(1)	rw–(0)	rw–(0)	rw–(0)	rw–0	rw–1	rw–0	rw–0

Bit0 to Bit2: The internal resistor is selected in eight different steps.
Rsel.0 to Rsel.2 The value of the resistor defines the nominal frequency.
The lowest nominal frequency is selected by setting Rsel=0.

Bit3, XT5V: XT5V should always be reset.

Bit4 to Bit5: The selected source for ACLK is divided by:
DIVA = 0: 1
DIVA = 1: 2
DIVA = 2: 4
DIVA = 3: 8

Bit6, XTS: The LFXT1 oscillator operates with a low-frequency clock crystal or with a high-frequency crystal:
XTS = 0: The low-frequency oscillator is selected.
XTS = 1: The high-frequency oscillator is selected.

The oscillator selection must meet the external crystal's operating condition.

Bit7, XT2Off: The XT2 oscillator is switched on or off:
XT2Off = 0: the oscillator is on
XT2Off = 1: the oscillator is off if it is not used for MCLK or SMCLK.

BCSCTL2 is affected by a valid PUC or POR condition.

BCSCTL2
058h

7							0
SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–0	rw–0	rw–0	rw–0

Bit0, DCOR: The DCOR bit selects the resistor for injecting current into the dc generator. Based on this current, the oscillator operates if activated.

DCOR = 0: Internal resistor on, the oscillator can operate. The fail-safe mode is on.

DCOR = 1: Internal resistor off, the current must be injected externally if the DCO output drives any clock using the DCOCLK.

Bit1, Bit2: The selected source for SMCLK is divided by:

DIVS.1 .. DIVS.0 DIVS = 0: 1
DIVS = 1: 2
DIVS = 2: 4
DIVS = 3: 8

Bit3, SELS: Selects the source for generating SMCLK:
SELS = 0: Use the DCOCLK
SELS = 1: Use the XT2CLK signal (in three-oscillator systems)
or
LFXT1CLK signal (in two-oscillator systems)

Bit4, Bit5: The selected source for MCLK is divided by:

DIVM.0 .. DIVM.1 DIVM = 0: 1
DIVM = 1: 2
DIVM = 2: 4
DIVM = 3: 8

Bit6, Bit7: Selects the source for generating MCLK:
SELM.0 .. SELM.1 SELM = 0: Use the DCOCLK
SELM = 1: Use the DCOCLK
SELM = 2: Use the XT2CLK (x13x and x14x devices) or
Use the LFXT1CLK (x11xx and x12xx devices)
SELM = 3: Use the LFXT1CLK

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