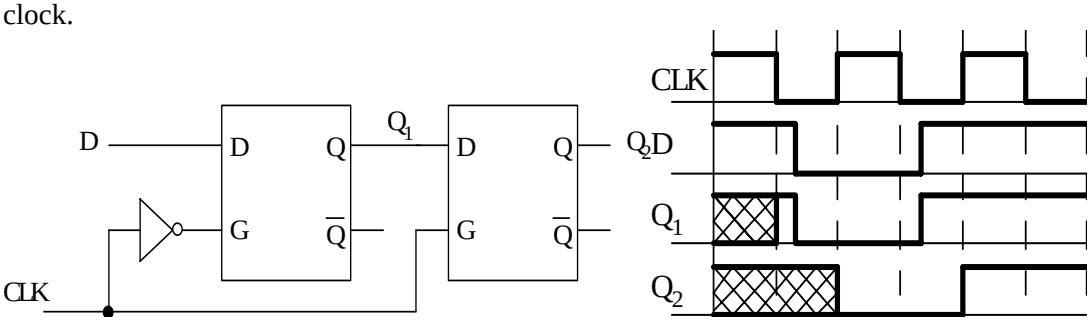
The University of Alabama in Huntsville
Electrical and Computer Engineering
CPE/EE 422/522
Spring 2005
Homework #2 Solution

1.7 (20 points) Construct a clocked D flip-flop, triggered on the rising edge of CLK, using two transparent D latches and any necessary gates. Complete the following timing diagram, where Q1 and Q2 are latch outputs. Verify that the flip-flop output changes to D after the rising edge of the clock.



1.8 (30 points) A synchronous sequential network has one input and one output. If the input sequence 0101 or 0110 occurs, an output of two successive 1s will occur. The first of these 1s should occur coincident with the last input of the 0101 or 0110 sequence. The network should reset when the second 1 output occurs. For example,

input sequence: `X = 010011101010 101101...`
output sequence: `Z = 000000000011 000000..`

(a) Derive a Mealy state graph and table with a minimum number of states (6 states).

	NS		Z	
PS	X = 0	X = 1	X = 0	X = 1
S0	S1	S0	0	0
S1	S1	S2	0	0
S2	S3	S4	0	0
S3	S1	S5	0	1
S4	S5	S0	1	0
S5	S0	S0	1	1

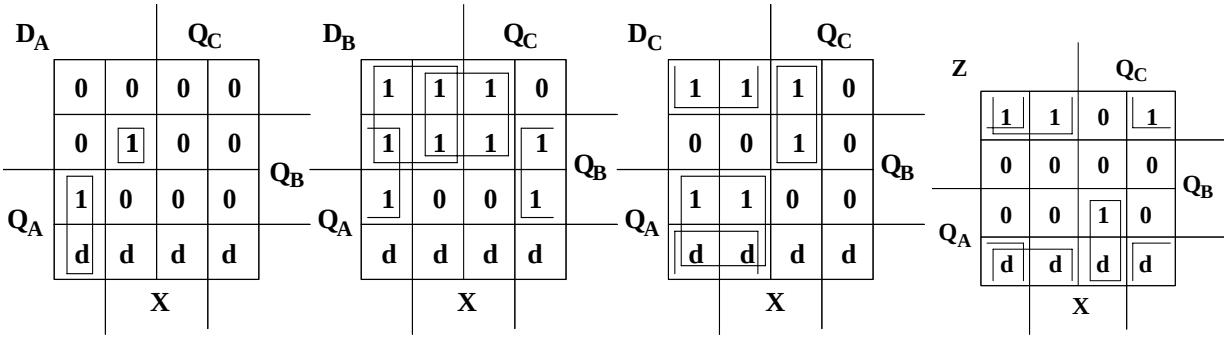
State Assignment Guidelines:

I {S0, S1,S3}{S0 ,S4, S5}
II {S0, S1}{S1, S2}{S3, S4}{S1, S5}{S0, S5}
III {S0, S1, S2}

			Q_B	
	S5	S4	S0	S1
Q_A			S3	S2
		Q_C		

S0 = 011, S1 = 010, S2 = 110, S3 = 111, S4 = 001, S5 = 000

	NS		Z	
PS	X = 0	X = 1	X = 0	X = 1
000	011	011	1	1
001	000	011	1	0
010	010	110	0	0
011	010	011	0	0
100	ddd	ddd	d	d
101	ddd	ddd	d	d
110	111	001	0	0
111	010	000	0	1



$$D_A = Q_A Q_B \overline{Q_C} X + Q_A \overline{Q_C}\,\overline{X}$$

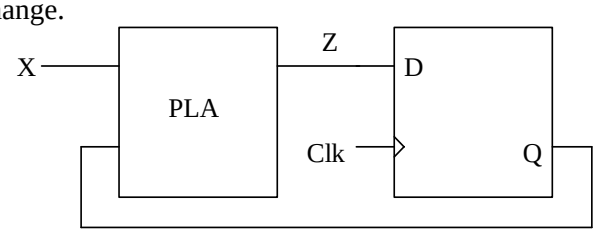
$$D_B = \overline{Q_A}\,\overline{Q_C} + \overline{Q_A} X + Q_B \overline{X}$$

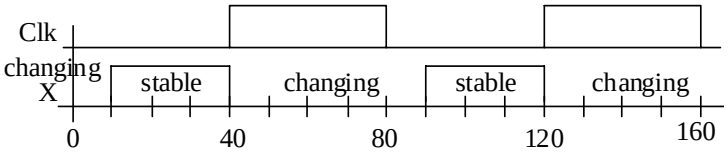
$$D_C = Q_A \overline{Q_C} + \overline{Q_B}\,\overline{Q_C} + \overline{Q_A} Q_C X$$

$$Z = \overline{Q_B}\,\overline{X} + \overline{Q_B}\,\overline{Q_C} X + Q_A Q_C X$$

(b) Try to choose a good state assignment. Realize the network using D flip-flops.

1.12 (25 points) A sequential network has the following form. The delay through the combinational network is in the range $5 \le t_c \le 20$ ns. The propagation delay from the rising edge of the clock to the change in the flip-flop output is in the range $5 \le t_p \le 10$ ns. The required setup and hold times for the flip-flop are $t_{su} = 10$ ns and $t_h = 5$ ns. Indicate on the diagram the times at which X is allowed to change.





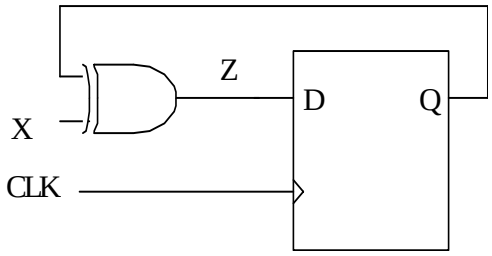
$t_x = t_{cmax} + t_{su} = 20$ ns + 10 ns = 30 ns

$t_y = t_h - t_{cmin} = 5$ ns – 5 ns = 0 ns

1.15 (25 points) A D flip-flop has a setup time of 4 ns, a hold time of 2 ns, and a propagation delay from the rising edge of the clock to the change in the flip-flop output in the range of 6 to 12 ns. The XOR gate dely is in the range of 1 to 8 ns.

(a) What is the minimum clock period for proper operation of the following network?

(b) What is the earliest time after the rising edge that X is allowed to change?



(a) $t_{ck} \geq t_{pmax} + t_{cmax} + t_{su}$

$t_{ck} \geq 12 \text{ ns} + 8 \text{ ns} + 4 \text{ ns}$

$t_{ck} \geq 24 \text{ ns}$

(b) $t_y = t_h - t_{cmin} = 2 \text{ ns} - 1 \text{ ns} = 1 \text{ ns}$