CPE/EE 422/522 SP2005, Lab Assignment 1

Decimal up-Counter

(Undergraduate 100 points – Graduate 80 points)

PART A (90/60 points)

The purpose of this laboratory project is to give each student the opportunity to develop a practical logic design using either schematic capture and/or VHDL that will implement a decimal up-counter that counts up to 99, using two four 4-bit binary counter developed in the previous lab and a modified bintohex file called bintodec. The result should display the decimal equivalent on the two Altera UP1 Educational Trainer's seven-segment LEDs.

PART B (10/20 points)

Add a reset button that clears the display and restarts the counter when pressed.

Pin Assignment

Altera Pin Numbers for the FLEX DIGIT Segment I/O Connections

FLEX_PB1 Push Button	28

Display Segment	Pin for Digit 1	Pin for Digit 2
A	6	17
B	7	18
C	8	19
D	9	20
E	11	21
F	12	23
G	13	24
Decimal	14	25

Lab Report Due Date 02/11/05 6pm