

CPE/EE 422/522 S2005, Laboratory Assignment 2

PS 2, PC Keyboard Interface

75/60 Points (422/522)

The purpose of this laboratory project is to give each student the opportunity to develop a practical logic design that interfaces a 104 key PS-2 style keyboard to the Altera UP 1 Educational Trainer. The design should be created in a manner that will allow it to display in hexadecimal format on two seven-segment LEDs, the final byte of the so-called make/break scan code sequence that is produced by the keyboard when each key is pressed.

Background

PS-2 type keyboards contain the embedded logic necessary to scan all 104 keys and produce a unique scan code for each key that is pressed. This logic performs a similar function to that which was performed by the scanning keypad design that was developed by CPE/EE 422/502 students in Laboratory Assignment 3. To greatly minimize the number of lines that connect the PS 2 keyboard to an external device (such as a PC, Altera UP-1, etc.) the embedded processor translates the scan code into a serial format. This effectively reduces the number of wires needed for a 104 key keyboard from 22 to about four, which include VCC, Ground, a keyboard clock, and a keyboard data line. The VCC and ground line are used to power the keyboard and data is transferred in and out of the keyboard using the bidirectional keyboard clock (KEY_CLK) and data (DATA) lines. In this lab, we will use the keyboard as an output only device meaning the from the digital design's point of view the keyboard clock and keyboard data lines are always inputs to the design. (It is possible, and common, for an external design to drive these lines in the other direction to perform such functions as resetting the keyboard, switching keyboards scan code character sets, etc. The keyboard is very flexible. We will only be using its basic default features in this laboratory assignment.)

In its default mode, every time a key is press a sequence of bytes is sent serially across the data line from the keyboard to the external device. There is a separate sequence of bytes that is sent when each key is pressed and another sequence that is sent when each key is released. The sequence that is sent when the key is pressed is often called the *Make Code* and the sequence that is sent when the key is released is called the *Break Code* . Except for a few special keys, the last byte that is sent in the make code and break code sequence for a given key are identical to one another with its value uniquely represents

the key that was pressed. Table 1 lists the final byte of the make/break sequences for each of the keys on the PS/2 keyboards that will be used in the laboratory assignment. This table assumes the key labeling that is shown in Figure 1.

Make/Break Codes for PS/2 Keyboard					
Key #	Final Byte of Make/Break Sequence	Key #	Final Byte of Make/Break Sequence	Key #	Final Byte of Make/Break Sequence
1	76	36	4A	71	6B
2	05	37	7C	72	73
3	06	38	7B	73	74
4	04	39	0D	74	79
5	0C	40	15	75	12
6	03	41	1D	76	1A
7	0B	42	24	77	22
8	83	43	2D	78	21
9	0A	44	2C	79	2A
10	01	45	35	80	32
11	09	46	3C	81	31
12	78	47	43	82	3A
13	07	48	44	83	41
14	7C	49	4D	84	49
15	7E	50	54	85	4A
16	77	51	5B	86	59
17	0E	52	5A	87	75
18	16	53	71	88	69
19	1E	54	69	89	72
20	26	55	7A	90	7A
21	25	56	6C	91	5A
22	2E	57	75	92	14
23	36	58	7D	93	1F
24	3D	59	58	94	11
25	3E	60	1C	95	29
26	46	61	1B	96	11
27	45	62	23	97	27
28	4E	63	2B	98	2F
29	55	64	34	99	14

30	5D	65	33	100	6B
31	66	66	3B	101	72
32	70	67	42	102	74
33	6C	68	4B	103	70
34	7D	69	4C	104	71
35	77	70	52		

Table 1

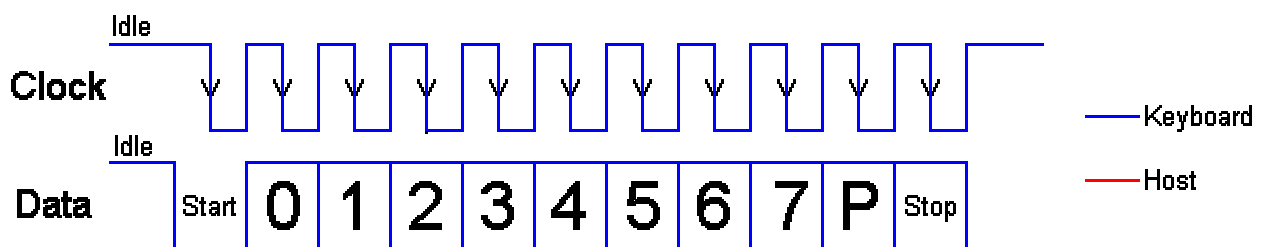


Figure 1

Each byte that is sent from the keyboard utilizes the keyboard clock and data lines, which are labeled, KEY_CLK and DATA, respectively, in the manner shown in Figure 2. If no external device force either of these lines to go low, then for each key pressed the keyboard will send each byte in the make/break byte sequence across the data line at a data transfer rate of approximately 14285 bits per second. It does this by first forcing the DATA line low to create a start bit and then initiating the keyboard clock sequence by first forcing the KEY_CLK line low for one half clock cycle. Information is then sent from the keyboard, with each bit being valid at the leading edge of each clock pulse. First the start bit is sent, then eight data bits, then a parity bit, and then a stop bit. After which the DATA and KEY_CLK lines are returned to the inactive state until the next byte is sent. Figure 2 illustrates the waveform that will appear when the keyboard sends out the value 76 hexadecimal (which corresponds to the last byte of the make/break code for key 1 shown in Figure 1 and Table 1).

The Altera UP 1 board supports the use of PS/2 devices with a standard PS/2 on-board connector. The connector is wired in a manner so that VCC and GND are connected to the appropriate pins of the PS/2 keyboard to power it up and the KEY_CLK, DATA lines are connected as shown in Table 2. For detailed connection information see page 13 of University Program Design Laboratory User Guide.

Altera Pin Numbers for the PS/2 Keyboard and Clock Lines	
Line	Pin Numbers
KEY_CLK	30
DATA	31

Assignment

A 60/40

All students are to develop a design that will display in hexadecimal the last byte of each make/break code sequence on two seven segment displays. There are to be two separate designs that are to be developed and demonstrated.

(30/20) I. Schematic capture based with only the binary to hexadecimal conversion sections of the design being implemented in VHDL.

(30/20) II. The second design should be entered entirely in VHDL.

Both designs must be demonstrated to the course or lab instructor and fully documented.

B 15/20

Develop an adder/subtractor of the make/break (Make – Break) codes displayed on the LEDs as decimals. Use the PB1 switch to enable the add/subtract option. Design should be done in VHDL.

Due 2-25-05 6pm NO late labs will be accepted. Early birds are welcomed