The University of Alabama in Huntsville
ECE Department
Course Syllabus
CPE 422/522 01
Spring 2005

Textbook: Digital Systems Design Using VHDL, Charles H. Roth, Jr., PWS Publishing, 1998 (ISBN: 0-534-95099-X)

Web Page: http://www.ece.uah.edu/courses/cpe422

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Lab Instructor: Preston Chidebelu, Office: EB 142, Phone: 824-6317, email: chidebp@ece.uah.edu

Office Hours: MW 2 PM – 3 PM, TR 4 PM – 5 PM, F 9 AM – 10 AM, or by appointment

Grading:

Homework	15 %
Lab Assignments	40 %
Midterm Exam	15 %
Final Exam	25 %
Class Attendance	5 %

Labs must be submitted at the beginning of the lab on the day they are due. Labs submitted more than one week late will not be graded. Late labs will be penalized 20 % for the first day late, and 10 % per day thereafter. No make-up exam will be given unless you make arrangements with the (lab) instructor at least 24 hours in advance. All requests for a re-grade must be submitted in writing within a week of the assignment being returned. No assignment will be re-graded after one week.

Any test done in pen will lose 10 %.

Attendance is calculated as follows: A student may miss up to 5 classes of the 28 classes in the semester and still receive all 5 points from attendance. If a student misses 6 or more classes, they receive 0 attendance points.

Lab Assignments: The laboratory assignment component of the grade will be composed of simulation, labs, practical exam, and, for graduate students, a separate graduate design project. SIMULATIONS represent small assignments, which utilize the ModelSim or Altera simulators to demonstrate the functionality of the design. The LABS represent complete digital designs, which are to be actually implemented on rapid prototyping hardware that is present in the Rapid Prototyping Laboratory (RPL). The practical EXAM is a short exam, which measures the student's ability to implement simple designs using the CAD tools. Graduate students will be given an additional graduate project (GRAD). The instructor will supply a default graduate laboratory assignment to the class. The assignment of credit for each of these components is shown below:

	CPE/EE 422	**CPE/EE 522**
1. Simulation	50 points	40 points
2. Lab #1	50 points	40 points
3. Lab #2	50 points	40 points
4. Lab #3	75 points	60 points
5. Lab #4	100 points	80 points
6. Lab Exam	75 points	65 points
7. Graduate Project	-	75 points

Homework: Homework turned in one class period late will be graded for 50 % credit; homework turned in more than one class period late will receive 0 % credit. Homework turned in more than 5 minutes into the class on the due date will incur a 5% deduction.

Academic Honesty: UAH is committed to the fundamental values of preserving academic honesty as defined in the Student Handbook (7.III.A). The instructor reserves the right to utilize electronic means to help prevent plagiarism. Students agree that by taking this course all assignments are subject to submission for textual similarity review to Turnitin.com. Assignments submitted to Turnitin.com will be included as source documents in Turnitin.com's restricted access database solely for the purpose of detecting plagiarism in such documents. The terms that apply to the University's use of the Turnitin.com service, as well as additional information about the company, are described at www.uah.edu/library/turnitin.

Important Dates: January 14 – Last day to add a class and file a course repeat
January 17 – Martin Luther King Holiday
January 24 – Last day to withdraw with refund
February 7 – Last day to change from credit to audit
March 21-26 – Spring Break
March 28 – Last day to withdraw
April 4 – Registration for Summer and Fall 2004 semesters begins
April 12 – Honors Day – No Classes
April 26 – Last TR class

Final Exam: May 3 – 8:00 AM – 10:30 AM

Miscellaneous: Mute your cell phones before you come to class.

Topics Covered

Chapter 1 Review of Logic Design Fundamentals
Combinational Logic, Boolean Algebra and Algebraic Simplification, Karnaugh Maps, Designing with NAND and NOR Gates, Hazards in Combinational Networks, Flip-flops and Latches, Mealy Sequential Network Design, Design of a Moore Sequential Network, Equivalent States and Reduction of State Tables, Sequential Network Timing, Setup and Hold Times, Synchronous Design, Tristate Logic and Busses

Chapter 2 Introduction to VHDL
VHDL Description of Combinational Networks, Modeling Flip-flops Using VHDL Processes, VHDL Models for a Multiplexer, Compilation and Simulation of VHDL Code, Modeling a Sequential Machine, Variables, Signals, and Constants, Arrays, VHDL Operators, VHDL Functions, VHDL Procedures, Packages and Libraries, VHDL Model for a 74163 Counter

Chapter 3 Designing with Programmable Logic Devices
Read-only Memories, Programmable Logic Arrays (PLAs), Programmable Array Logic (PALs), Other Sequential Programmable Logic Devices (PLDs), Design of a Keypad Scanner

Chapter 4 Design of Networks for Arithmetic Operations
State Graphs for Control Networks, Design of a Binary Multiplier,

Chapter 5 Digital Design With SM Charts
State Machine Charts, Derivation of SM Charts, Realization of SM Charts, Implementation of the Dice Game

Chapter 6 Designing With Programmable Gate Arrays and Complex Programmable Logic Devices
Xilinx 3000 Series FPGAs, Designing with FPGAs, Xilinx 4000 Series FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs

Chapter 8 Additional Topics in VHDL
Attributes, Transport and Inertial Delays, Operator Overloading, Multivalued Logic and Signal Resolution, IEEE-1164 Standard Logic, Generics, Generate Statements, Synthesis of VHDL Code, Synthesis Examples, Files and TEXTIO

Chapter 10 Hardware Testing and Design for Testability
Testing Combinational Logic, Testing Sequential Logic, Scan Testing, Boundary Scan, Built-In Self-Test

Tentative Course Schedule:

Date		Topic	Homework Due
1/11	T	Introduction, 1.1, 1.2	
1/13	R	1.3, 1.4, 1.13	
1/18	T	3.1, 3.2, 3.3	
1/20	R	1.6, 1.7	
1/25	T	1.7, 1.8	#1
1/27	R	1.10, 1.11, 1.12	
2/1	T	1.9, 1.5	#2
2/3	R	2.1, 2.2	
2/8	T	2.3, 2.4	#3
2/10	R	2.4, 2.5	
2/15	T	2.5, 2.6	#4
2/17	R	2.7, 2.8	
2/22	T	2.9, 2.10	#5
2/24	R	Midterm	
3/1	T	2.11, 2.12	
3/3	R	3.4, 6.1	
3/8	T	6.2	#6
3/10	R	6.3	
3/15	T	6.4, 6.5	#7
3/17	R	6.6	
3/22	T	Spring Break – No Class	
3/24	R	Spring Break – No Class	
3/29	T	8.1, 8.2, 8.3	
3/31	R	8.4, 8.5	
4/5	T	8.6, 8.7	#8
4/7	R	8.8, 8.9	
4/12	T	Honors Day – No Class	
4/14	R	4.2, 4.3, 5.1, 5.2	
4/19	T	10.1, 10.2, 10.3	#9
4/21	R	10.4, 10.5	
4/26	T	Review	
5/3	T	Final Exam	

I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook while I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

Name (Printed)	Signature	Date