

The University of Alabama in Huntsville
Electrical and Computer Engineering
CPE/EE 422/522
Spring 2004
Homework #2 Solution

- 1.8 A synchronous sequential network has one input and one output. If the input sequence 0101 or 0110 occurs, an output of two successive 1s will occur. The first of these 1s should occur coincident with the last input of the 0101 or 0110 sequence. The network should reset when the second 1 output occurs. For example,

input sequence: $X = 010011101010 \ 101101\dots$

output sequence: $Z = 000000000011 \ 000000\dots$

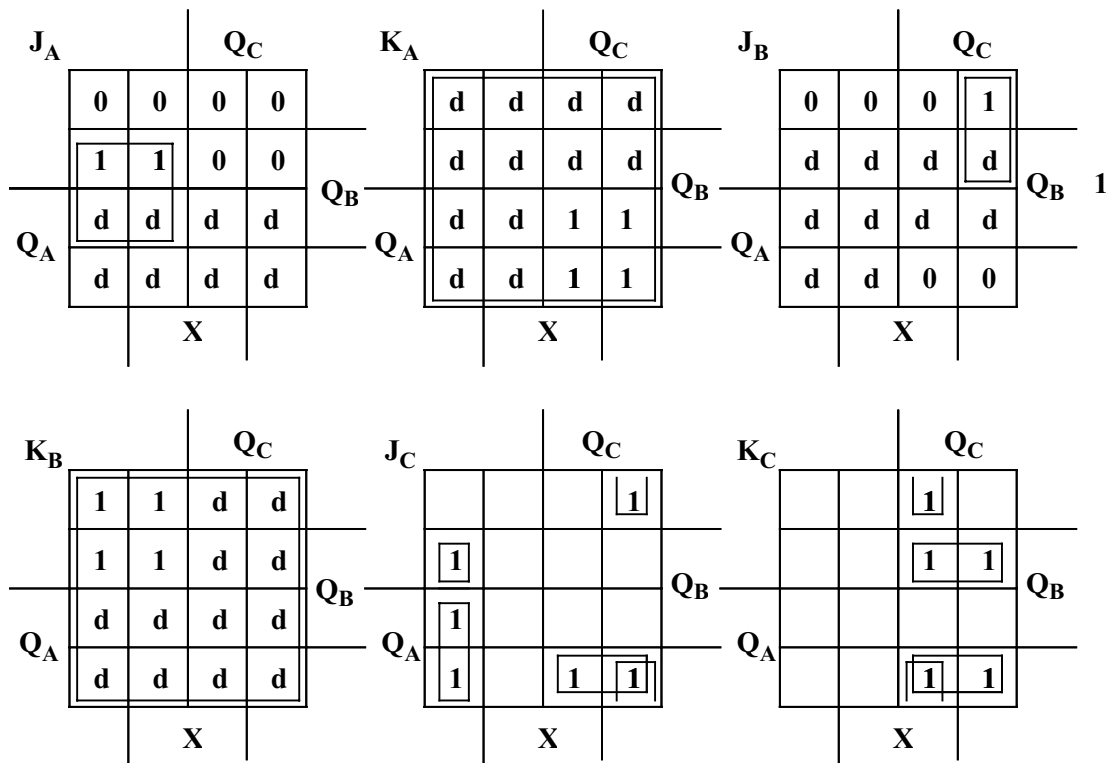
(a) Derive a Mealy state graph and table with a minimum number of states (6 states).

	NS		Z	
PS	X = 0	X = 1	X = 0	X = 1
S0	S1	S0	0	0
S1	S1	S2	0	0
S2	S3	S4	0	0
S3	S1	S5	0	1
S4	S5	S0	1	0
S5	S0	S0	1	1

State Assignment Guidelines:

- I {S0, S1, S3} {S0, S4, S5}
- II {S0, S1} {S1, S2} {S3, S4} {S1, S5} {S0, S5}
- III {S0, S1, S2}

	NS		Z		JaKa		JbKb		JcKc	
PS	X = 0	X = 1	X = 0	X = 1	X = 0	X = 1	X = 0	X = 1	X = 0	X = 1
000	001	001	1	1	0d	0d	0d	0d	1d	1d
001	011	001	0	0	0d	0d	1d	0d	D0	D0
010	111	101	0	0	1d	1d	D0	D1	1d	1d
011	011	010	0	0	0d	0d	D0	D0	D0	D1
100	ddd	ddd	D	D	Dd	Dd	Dd	Dd	Dd	Dd
101	000	001	1	0	D1	D1	0d	0d	D1	D0
110	ddd	ddd	D	D	Dd	Dd	Dd	Dd	Dd	Dd
111	011	000	0	1	D1	D1	D0	D1	D0	D1



$$\begin{aligned}
 J_A &= Q_B \overline{Q_C} \\
 K_A &= 1 \\
 J_B &= \overline{Q_A} Q_C \overline{X} \\
 K_B &= Q_A X + \overline{Q_C} X \\
 J_C &= 1 \\
 K_C &= Q_B X + Q_A \overline{Q_B} \overline{X} \\
 Z &= \overline{Q_B} \overline{Q_C} + Q_A Q_B X + Q_A \overline{Q_B} \overline{X}
 \end{aligned}$$

(b) Try to choose a good state assignment. Realize the network using J-K flip-flops and NAND gates. Repeat using NOR gates.

- 1.10 A sequential network has one input (X) and two outputs (S and V). X represents a 4-bit binary number N, which is input least significant first. S represents a 4-bit binary number equal to N + 2, which is output least significant bit first. At the time the fourth input occurs, V = 1 if N + 2 is too large to be represented by 4 bits; otherwise, V = 0. The value of S should be the proper value, not a don't care, in both cases. The network always resets after the fourth bit of X is received.

X	S	V
0000	0010	0
0001	0011	0
0010	0100	0
0011	0101	0
0100	0110	0

0101	0111	0
0110	1000	0
0111	1001	0
1000	1010	0
1001	1011	0
1010	1100	0
1011	1101	0

1100	1110	0
1101	1111	0
1110	0000	1
1111	0001	1

	NS		SV	
PS	X = 0	X = 1	X = 0	X = 1
S0	S1	S1	00	10
S1	S2	S3	10	00
S2	S4	S4	00	10
S3	S4	S5	10	00
S4	S0	S0	00	10
S5	S0	S0	11	01

State Assignment Guidelines

- I {S4, S5}
- II {S2, S3}{S4, S5}
- III {S0, S2, S4}{S1, S3}

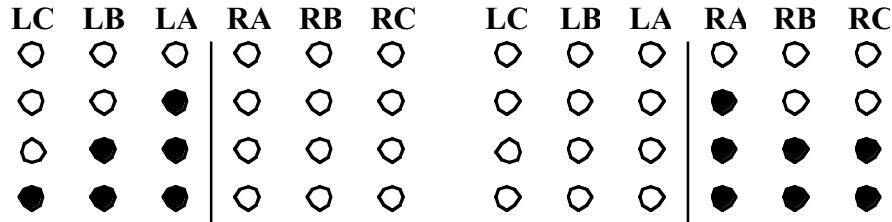
	NS		SV		JaKa		JbKb		JcKc	
PS	X = 0	X = 1	X = 0	X = 1	X = 0	X = 1	X = 0	X = 1	X = 0	X = 1
000	110	110	00	10	1d	1d	1d	1d	0d	0d
110	101	100	10	00	d0	d0	d1	d1	1d	0d
101	001	001	00	10	d1	d1	0d	0d	d0	d0
100	001	011	10	00	d1	d1	0d	0d	1d	1d
001	000	000	00	10	0d	0d	0d	0d	d1	d1
011	000	000	11	01	0d	0d	1d	1d	d1	d1

$$\begin{aligned}
 J_A &= \overline{Q_C} \\
 K_A &= \overline{Q_B} \\
 J_B &= Q_B + \overline{Q_A} \overline{Q_C} \\
 K_B &= \overline{Q_B} \\
 J_C &= \overline{Q_A} \overline{Q_B} + Q_A \overline{X} \\
 K_C &= \overline{Q_A} \\
 S &= \overline{Q_A} \overline{Q_B} X + Q_B \overline{Q_C} \overline{X} + Q_A \overline{Q_C} \overline{X} + Q_A Q_C X \\
 V &= Q_B Q_C
 \end{aligned}$$

3.2 An older-model Thunderbird car has three left and three right tail lights, which flash in unique patterns to indicate left and right turns.

Left-turn pattern:

Right-turn pattern:



Design a Moore sequential network to control these lights. The network has three inputs, LEFT, RIGHT, and HAZ. LEFT and RIGHT come from driver's turn-signal switch and cannot be 1 at the same time. As indicated above, when LEFT = 1, the lights flash in a pattern LA on, LA and LB on, LA, LB, and LC on and all off; then the sequence repeats. When RIGHT = 1, the light sequence is similar. IF a switch from LEFT to RIGHT (or vice versa) occurs in the middle of a flashing sequence, the network should immediately go to the IDLE state (lights off) and then start the new sequence. HAZ comes from the hazard switch, and when HAZ = 1, all six lights flash on and off in unison. HAZ takes precedence if LEFT or RIGHT is also on. Assume that a clock signal is available with a frequency equal to the desired flashing rate.

- Draw the state graph (8 states).
- Realize the network using D flip-flops, and make a state assignment such that each flip-flop output drives one of the six lights directly.
- Realize the network using three D flip-flops, using the guidelines to determine a suitable state assignment.

		D _{LC}	D _{LB}	D _{LA}	D _{RA}	D _{RB}	D _{RC}
S0 — IDLE	S0	0	0	0	0	0	0
S1 — RA	S1	0	0	0	1	0	0
S2 — RA, RB	S2	0	0	0	1	1	0
S3 — RA, RB, RC	S3	0	0	0	1	1	1
S4 — LA	S4	0	0	1	0	0	0
S5 — LA, LB	S5	0	1	1	0	0	0
S6 — LA, LB, LC	S6	1	1	1	0	0	0
S7 — LC, LB, LA, RA, RB, RC	S7	1	1	1	1	1	1

(a)

	NS			
PS	LRH = 000	LRH = 010	LRH = 100	LRH = dd1
S0	S0	S1	S4	S7
S1	S0	S2	S0	S0
S2	S0	S3	S0	S0
S3	S0	S0	S0	S0
S4	S0	S0	S5	S0
S5	S0	S0	S6	S0
S6	S0	S0	S0	S0
S7	S0	S0	S0	S0

$$D_{LC} = \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} \overline{D_{RC}} LRH + \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} D_{RC} H$$

$$D_{LB} = D_{LC} + \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} D_{RC} LRH$$

$$\begin{aligned}
D_{LA} &= D_{LB} + \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} \overline{D_{RC}} \overline{LRH} \\
D_{RC} &= \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} \overline{D_{RC}} \overline{LRH} + \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} \overline{D_{RC}} H \\
D_{RB} &= D_{RC} + \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} \overline{D_{RC}} \overline{LRH} \\
D_{RA} &= D_{RB} + \overline{D_{LC}} \overline{D_{LB}} \overline{D_{LA}} \overline{D_{RA}} \overline{D_{RB}} \overline{D_{RC}} \overline{LRH}
\end{aligned}$$

PS	LRH = 000	LRH = 010	LRH = 100	LRH = dd1
000 000	000 000	000 100	001 000	111 111
000 100	000 000	000 110	000 000	000 000
000 110	000 000	000 111	000 000	000 000
000 111	000 000	000 000	000 000	000 000
001 000	000 000	000 000	011 000	000 000
011 000	000 000	000 000	111 000	000 000
111 000	000 000	000 000	000 000	000 000
111 111	000 000	000 000	000 000	000 000

State Assignment Guidelines:

- I {S0, S1, S2, S3, S4, S5, S6, S7} {S3, S4, S5, S6, S7} {S1, S2, S3, S6, S7} {S1, S2, S3, S4, S5, S6, S7}
- II {S1, S4, S7} {S0, S2} {S0, S3} {S0, S5}
- III {S3, S6, S7}

	NS			
PS	LRH = 000	LRH = 010	LRH = 100	LRH = dd1
100	100	000	010	011
000	100	001	100	100
001	100	101	100	100
101	100	100	100	100
010	100	100	110	100
110	100	100	111	100
111	100	100	100	100
011	100	100	100	100

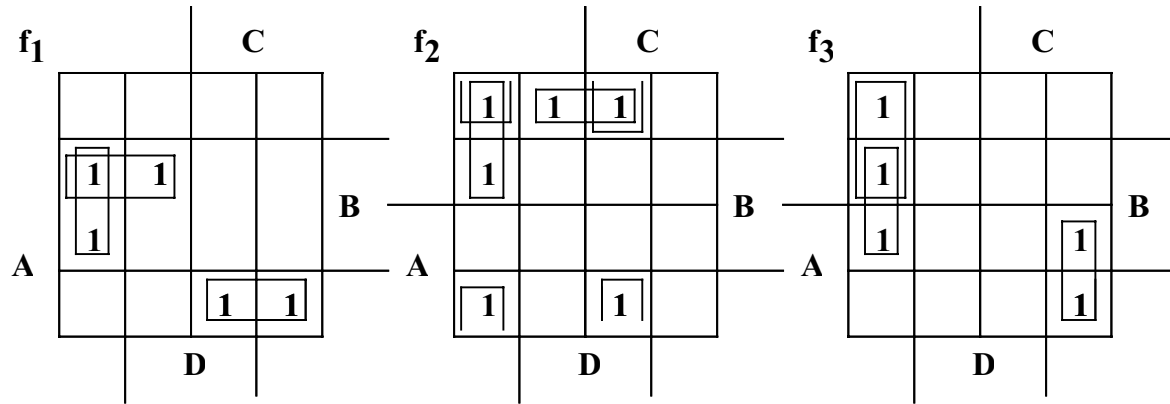
$$\begin{aligned}
\overline{Q_A} &= \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} H \\
Q_B &= \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} H \\
Q_C &= \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} \overline{LRH} + \overline{Q_A} \overline{Q_B} \overline{Q_C} H \\
L_C &= \overline{Q_B} \overline{Q_C} \\
L_B &= \overline{Q_B} \overline{Q_C} + \overline{Q_A} \overline{Q_B} \\
L_A &= \overline{Q_B} \\
R_A &= \overline{Q_A} \overline{Q_B} + \overline{Q_B} \overline{Q_C} + \overline{Q_A} \overline{Q_C} \\
R_B &= \overline{Q_B} \overline{Q_C} + \overline{Q_A} \overline{Q_C} \\
R_C &= \overline{Q_A} \overline{Q_B} \overline{Q_C} + \overline{Q_A} \overline{Q_B} \overline{Q_C}
\end{aligned}$$

3.3 Find a minimum-row PLA table to implement the following sets of functions.

(a) $f_1(A, B, C, D) = \Sigma m(4, 5, 10, 11, 12)$

$f_2(A, B, C, D) = \Sigma m(0, 1, 3, 4, 8, 11)$

$f_3(A, B, C, D) = \Sigma m(0, 4, 10, 12, 14)$



$$f_1 = \overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C}$$

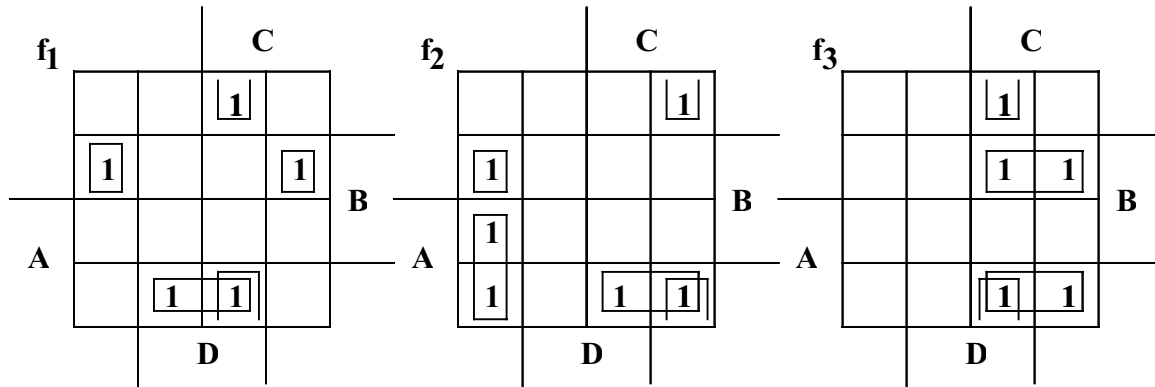
$$f_2 = \overline{A}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D}$$

$$f_3 = \overline{B}\overline{C}\overline{D} + \overline{A}\overline{C}\overline{D} + \overline{A}\overline{C}\overline{D}$$

(b) $f_1(A, B, C, D) = \Sigma m(3, 4, 6, 9, 11)$

$f_2(A, B, C, D) = \Sigma m(2, 4, 8, 10, 11, 12)$

$f_3(A, B, C, D) = \Sigma m(3, 6, 7, 10, 11)$



$$f_1 = \overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D}$$

$$f_2 = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{C}\overline{D} + \overline{B}\overline{C}\overline{D}$$

$$f_3 = \overline{A}\overline{B}\overline{C} + \overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}$$