**The University of Alabama in Huntsville**
**ECE Department**
**CPE 526 01**
**Final Exam**
**December 3, 2007**

Name: _____

1. (5 points) Draw the transistor-level diagram of a two-input CMOS NAND gate.

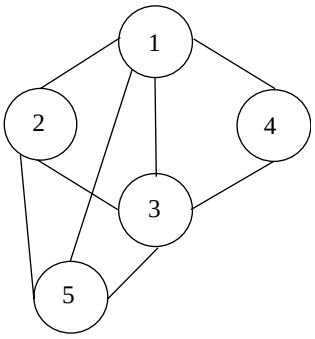
2. (10 points) Write a VHDL entity (3 points) and architecture (7 points) of a D latch with the generics, TPDQ, which reflects the time for a change on D to appear at the outputs and TGDQ, which reflects the time for a change on the gate input, D, to appear at the outputs.

3. (1 point) _____ consists of assigning each operation to a control step.

4. (1 point) The _____ of a component is the ratio of the busy time for the component to the execution time for the process.

5. (4 points) If the NRE costs for FPGA and ASIC circuits are $25,000 and $575,000, respectively, and the cost of individual parts for FPGA and ASIC circuits are $22 and $7, respectively, what is the break-even manufacturing volume for these two types of circuits?

6. (10 points) Consider the dataflow graph shown below. As part of the cluster partitioning algorithm, determine which two nodes should be merged and show the dataflow graph that results from the merger.




7. (4 points) List the four types of paths that must be considered when doing timing analysis of sequential circuits.

_____

_____

_____

_____

8. (1 point ) _____ is the process of transforming a behavioral description into a structural gate-level circuit.

9. (1 point) _____ is the process of making the connections between standard cells.

10. (10 points) For the data lifetime chart shown, use the left edge algorithm to obtain an efficient register allocation.

| | A | B | C | D | E | F | G | H | I | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S1 | | | | X | | | X | | | X | | |
| S2 | X | | | X | | | X | | X | X | | |
| S3 | X | X | | X | | X | | | X | X | X | |
| S4 | X | X | | X | | X | | X | X | | X | |
| S5 | X | X | | | X | X | | X | | | X | X |
| S6 | | X | X | | X | X | | X | | | | X |
| S7 | | | X | | | | | | | | | X |

11. (5 points) Translate the following VHDL use (a) block statement(s) instead of a process:

```
process (S1, S4, DI, S3, Q)
  begin
    if (S1 = '1' and S4 = '1') then
      Q <= DI after FFDEL;
    elsif (S1 = '0' and S4 = '0') then
      Q <="00000000" after FFDEL;
    end if;
    if (S3 = '1') then
      DO <= Q after BUFDEL;
    else
      DO <= "ZZZZZZZZ" after BUFDEL;
    end if;
```

12. (8 points) (a) (5 points) Write a single VHDL model which represents an AND gate with an arbitrary number of inputs, N. (b) (3 points) Use that model as a component in an entity that represents a four input AND gate with inputs a, b, c, d and output f

13. (10 points) A sequential network with one input and one output is used to stretch the first two bits of a 4-bit sequence as follows:

| Input | Output |
|---|---|
| 00dd | 0000 |
| 01dd | 0011 |
| 10dd | 1100 |
| 11dd | 1111 |

After every four bits, the network resets. Model this network in VHDL as a Moore state machine.
a. (3 points) Write an entity. b. (7 points) Write an architecture.

Consider the following VHDL code:

```
--------------------------------------
-- Entity declaration
--------------------------------------

entity SCHED2 is
  port (A, B, C, D, E, F: in INTEGER;
        CLK : in BIT;
        W, X, Y: out INTEGER);
end SCHED2;

--------------------------------------
-- Architecture declaration
--------------------------------------

architecture HIGH_LEVEL of SCHED2 is
  signal V, Z: INTEGER;
begin
  X <= ((A – B) * Z) * (C + V);
  Y <= ((A * B) + Z) * E + F;
  Z <= (C * D) + D * (E + F);
  W <= (A/F + C*C + D* (A – B))/V;
  V <= (C * (B + D*E)) + F;
end HIGH_LEVEL;
```

16. (10 points) The following task refers to the VHDL code above. Assume that all operations are done in an ALU module and there are two ALU modules available. Derive a list schedule using the critical path priority metric for the operations.

17. (10 points) Write a VHDL model for a shift register module that includes a 16-bit shift register, a controller, and a 4-bit down counter. The shifter can shift a variable number of bits depending on a count provided to the shifter module. Inputs to the module are a number N (indicating a shift count) in the range 1 to 15, a 16-bit vector par_in, a clock and a start signal, St. When St = '1', N is loaded in the down counter, and par_in is loaded into the shift register. Then the shift register does a left shift N times and the controller returns to the start state. Assume that St is only '1' for one clock time. All operations are synchronous on the falling edge of the clock.

18. (10 points) A Mealy sequence detector detects a sequence of four consecutive 1 inputs. The detector has a single binary input, X, and a single binary output, Z. Signal Z should be logic 1 if and only if the last four inputs were all logic 1. Here is an example input-output sequence:

    X  01011111101101011110
    Z  00000011110000000010

    Model this detector in VHDL.