1. (20 points) Describe the following logic expression

$$(A' \bullet B' \bullet D) + (A \bullet B \bullet C) + (B' \bullet C')$$

with a structural VHDL model using the following package located in library WORK.

Hint: If you don't need all of the inputs, you can tie one or more of them to '0' or '1'.

```
package LOGIC_PKG is
  component AND2_OP
    port (A, B : in BIT; Z out BIT);
  end component;
  component NOR2_OP
    port (A, B : in BIT; Z out BIT);
  end component;
  component OR4_OP
    port (A, B, C, D : in BIT; Z out BIT);
  end component;
end LOGIC_PKG;
```

2. (10 points) Write a procedure that accepts a `std_logic_vector` of arbitrary length and returns an integer which represents the total number of '1's contained in the `std_logic_vector` and an integer which represents the total number of '0's contained in the `std_logic_vector`.

3. (2 points) List two of the three primary design units in VHDL

_____

_____

4. (1 point) _____ delay is the delay which represents gate delay in VHDL.

5. (1 point) _____ (True or False) All sequential statements are synthesized into sequential circuits.

6. (1 point) A top-level entity designed to test a VHDL model is called a _____.

7. (20 points) Consider the following combinational digital system, a priority encoder. In a priority encoder, each input has a priority level associated with it. The encoder outputs indicate the active input that has the highest priority. When an input with a high priority is asserted, the other inputs with lower priority are ignored. The truth table for a 4-2 priority encoder is shown below. It assumes that w_0 has the lowest priority and w_3 the highest. The outputs y_1 and y_0 represent the binary number that identifies the highest priority input set to 1. Since it is possible that none of the inputs is equal to 1, an output, z, is provided to indicate this condition. It is set to 1 when at least one of the inputs is equal to 1, and 0 otherwise. d – don't care
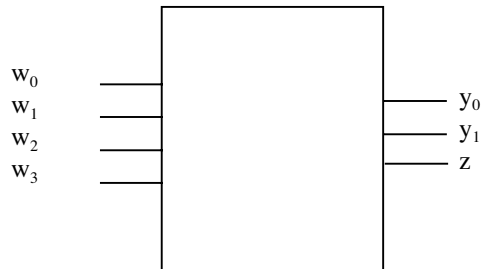
w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	d	0	1	1
0	1	d	d	1	0	1
1	d	d	d	1	1	1

Inputs: w_0, w_1, w_2, w_3
Outputs: y_0, y_1, z

 (a) (4 points) Write an entity for the priority encoder.
(b) (8 points) Use concurrent signal assignments to model the priority encoder.
(c) (8 points) Use a process statement and sequential statements to model the priority encoder.

8. (10 points) Write a VHDL description for a rising D-type edge-triggered flip-flop with synchronous set and reset inputs active high and two outputs. Label the data, clock, set and reset inputs, d, c, s, and r, respectively. s and r cannot simultaneously be active.

    a. (3 points) Write an entity.

    b. (7 points) Write a synthesizable behavioral architecture.

9. (1 point) A process is triggered whenever a signal in its _____ has an event on it.

10. (1 point) _____ (True or False) It is possible to make aggregate assignments in VHDL.

11. (1 point) _____(True or False) Multiple assignments to a signal within a process can cause that signal to have multiple drivers.

12. (1 point) _____(True or False) A D flip-flop and a D latch have the same behavior.

13. (1 point) 'RANGE is an example of a VHDL _____.

14. (20 points) Specify type declarations for the following data types.

a. (3 points) A seven valued logic system, MVL7, with values '0', '1', 'X', 'Z', 'U', 'L', and 'H'. Values '0' and '1' have the usual logic meaning. Value 'Z' means high impedance state, 'X' means unknown, 'U' means uninitialized ,'L' means a weak 0 and 'H" means a weak 1. Any uninitialized data item of this type should have the value 'U'.

b. (3 points) A COLORS_OF_THE_RAINBOW enumeration data type.

c. (2 points) A data type REGISTER_NUMBER that can have integer values in the range from 0 to 31.

d. (2 points) A data type TAX that can have real values between $0.00 and $9,999.99.

e. (2 points) An ascending range data type ASC_32 with integer values from 0 to 31.

f. (4 points) A 16-bit ascending-index register composite data type, REG_32_ASCENDING, with index valued from the type ASC_32 declared above, and component values of type MVL7.

g. (4 points) A three-dimensional table, TABLE_3D, with first and second indices of type REGISTER_NUMBER, and third index of type BOOLEAN and table entries type COLORS_OF_THE_RAINBOW.

15. (10 points) Draw the state diagram for the following state machine. Is it a Moore machine or a Mealy machine?

```vhdl
ENTITY state_machine IS
    PORT (Clock, Resetn ; IN BIT;
          r               : IN BIT_VECTOR(1 to 3);
          g               : OUT BIT_VECTOR(1 to 3));
END state_machine;

ARCHITECTURE behavior OF state_machine IS
    TYPE state_type IS (Idle, gnt1, gnt2, gnt3);
    SIGNAL y : state_type;
BEGIN
    PROCESS (Resetn, Clock)
    BEGIN
        IF (Resetn = '0') THEN
            y <= Idle;
        ELSIF (Clock' EVENT AND Clock = '1') THEN
            CASE y IS
                WHEN Idle =>
                    IF (r(1) = '1') THEN
                        y <= gnt1;
                    ELSIF (r(2) = '1') THEN
                        y <= gnt2;
                    ELSIF (r(3) = '1') THEN
                        y <= gnt3;
                    ELSE
                        y <= Idle;
                    END IF;
                WHEN gnt1 =>
                    IF (r(1) = '1') THEN
                        y <= gnt1;
                    ELSE
                        y <= Idle;
                    END IF;
                WHEN gnt2 =>
                    IF (r(2) = '1') THEN
                        y <= gnt2;
                    ELSE
                        y <= Idle;
                    END IF;
                WHEN gnt3 =>
                    IF (r(3) = '1') THEN
                        y <= gnt3;
                    ELSE
                        y <= Idle;
                    END IF;
            END CASE;
        END IF;
    END PROCESS;

    g(1) <= '1' WHEN y = gnt1 ELSE '0';
    g(2) <= '1' WHEN y = gnt2 ELSE '0';
    g(3) <= '1' WHEN y = gnt3 ELSE '0';

END behavior;
```