CPE 426 Spring 2003 Midterm Solutions:

1.

```
USE WORK.logic_pkg.ALL;

entity LOGIC is
  port (A, B, C, D : in BIT;
                F : out BIT);
end LOGIC;

architecture LOGIC of LOGIC is
   signal ABAR, BBAR, CBAR : BIT;
   signal TEMP : BIT_VECTOR (1 to 5);
begin
  U1 : NOR2_OP port map(A, A, ABAR);
  U2 : NOR2_OP port map(B, B, BBAR);
  U3 : NOR2_OP port map(C, C, CBAR);
  U4 : AND2_OP port map(BBAR, CBAR, TEMP(1));
  U5 : AND2_OP port map(ABAR, BBAR, TEMP(2));
  U6 : AND2_OP port map(TEMP(2), D, TEMP(3));
  U7 : AND2_OP port map(A, B, TEMP(4));
  U8 : AND2_OP port map(C, TEMP(4), TEMP(5));
  U9 : OR4_OP port map(TEMP(1), TEMP(3), TEMP(5), '0', F);
end LOGIC;
```

2. (1 point) A process is triggered whenever a signal in its
____sensitivity list___ has an event on it.

3. (2 points) List two of the three primary design units in VHDL
_entity_____________
_package_____________
_configuration_____

4. (1 point) _Inertial__ delay is the delay which represents gate delay in VHDL.

5. (1 point) _FALSE_ (True or False) All sequential statements are synthesized into sequential circuits.

6. (1 point) A top-level entity designed to test a VHDL model is called a _test bench__.

7.

```
entity DFF_SYNCH_RS is
  port (D, C, R, S : in BIT;
              Q, QB : out BIT);
end DFF_SYNCH_RS;

architecture DFF_SYNCH_RS of DFF_SYNCH_RS is
begin
   process (C)
   begin
      if (C = '1' and C'EVENT) then
         if (S = '1') then
            Q <= '1';
            QB <= '0';
```

```
         elsif (R = '1') then
            Q <= '0';
            QB <= '1';
         else
            Q <= D;
            QB <= not D;
         end if;
      end if;
   end process;
end DFF_SYNCH_RS;
```

8.
```
entity PRIORITY_ENCODER is
   port (W : in BIT_VECTOR (3 downto 0);
         Y : out BIT_VECTOR (1 downto 0);
         Z : out BIT);
end PRIORITY_ENCODER;

architecture SEQ of PRIORITY_ENCODER is
begin
   process (W)
   begin
      Z <= '1';
      if (W(3) = '1') then
         Y <= "11";
      elsif (W(2) = '1') then
         Y <= "10";
      elsif (W(1) = '1') then
         Y <= "01";
      elsif (W(0) = '1') then
         Y <= "00";
      else
         Z <= '0';
      end if;
   end process;
end SEQ;

architecture CON of PRIORITY_ENCODER is
begin
   Z <= '0' when W = "0000" else
        '1';
   Y <= "11" when W(3) = '1' else
        "10" when W(2) = '1' else
        "01" when W(1) = '1' else
        "00" when W(0) = '1';
end CON;
```

9. (1 point) _TRUE_ (True or False) It is possible to make aggregate assignments in VHDL.

10. (1 point) _FALSE_(True or False) Multiple assignments to a signal within a process can cause that signal to have multiple drivers.

11. (1 point) _FALSE_(True or False) A D flip-flop and a D latch have the same behavior.

12. (1 point) ‘RANGE is an example of a VHDL _attribute__.

13.

```
package TEST_TYPES is
  type MVL7 is ('U', 'L', 'H', 'X', 'Z', '0', '1');
  type COLORS_OF_THE_RAINBOW is (RED, ORANGE, YELLOW,
                       GREEN, BLUE, INDIGO, VIOLET);
  subtype REGISTER_NUMBER is integer range 0 to 31;
  subtype TAX is real range 0.0 to 9999.99;
  subtype ASC_32 is integer range 0 to 31;
  type REG_32_ASCENDING is array (ASC_32) of MVL7;
  type TABLE_3D is array (ASC_32, ASC_32, BOOLEAN)
                   of COLORS_OF_THE_RAINBOW;
end TEST_TYPES;
```

14.

Inputs		Present State			
	Idle	gnt1	gnt2	gnt3	
Reset,r					
0ddd	Idle	Idle	Idle	Idle	
1000	Idle	Idle	Idle	Idle	
1001	gnt3	Idle	Idle	gnt3	N S
1010	gnt2	Idle	gnt2	Idle	e t
1011	gnt2	Idle	gnt2	gnt3	x a
1100	gnt1	gnt1	Idle	Idle	t t
1101	gnt1	gnt1	Idle	gnt3	e
1110	gnt1	gnt1	gnt2	Idle	
1111	gnt1	gnt1	gnt2	gnt3	
output	000	100	010	100	

d - don't care