

The University of Alabama in Huntsville
ECE Department
CPE 426 01
Final Exam
April 29, 2004

Name: _____

Posting Code: _____

1. (7 points) Draw the transistor-level diagram of a CMOS two-input NOR gate.
2. (10 points) Write a VHDL entity (3 points) and architecture (7 points) of a two-input OR gate with the generics, TPLH and TPHL, which reflect the time for the output to make a low to high or high to low transition, respectively.

3. (1 point) _____ is the process of making the connections between standard cells.

4. (5 points) If the NRE costs for FPGA and CBIC circuits are \$21,000 and \$187,000, respectively, and the cost of individual parts for FPGA and CBIC circuits are \$15 and \$7, respectively, what is the break-even manufacturing volume for these two types of circuits?

5. (5 points) What kind of hardware element will be inferred by a synthesis tool from the following model?

```
library ieee;
use ieee.std_logic_1164.all;

entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK, RESET : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;

architecture EXAMPLE of WIDGET is
begin
  process (CLK, RESET)
  begin
    if (CLK'event and CLK = '1') then
      if (RESET = '1') then
        Z <= '0';
      else
        Z <= A nor B;
      end if;
    end if;
  end process;
end EXAMPLE;
```

6. (10 points) For the data lifetime chart shown, use the left edge algorithm to obtain an efficient register allocation.

	A	B	C	D	E	F	G	H	I	J	K	L
S1			X	X			X					
S2		X	X				X			X		
S3		X				X	X		X	X	X	
S4	X	X				X			X		X	X
S5	X				X	X		X	X		X	X
S6	X				X			X	X			X
S7					X				X			X

7. (1 point) Typically, a _____ is developed to validate a VHDL behavioral model.

8. (1 point) A(n) _____ provides the gate-level circuit with accurate timing backannotated from the layout.

9. (1 point) _____ are inserted into VHDL models to give instructions to synthesis or other tools.

10. (18 points) Create a VHDL entity named `en_dec_328` that represents a 3-to-8 decoder with an active-low enable input which has an architecture which uses a case statement to represent the functionality of the decoder. Create a second entity and its accompanying architecture that represents a 4-to-16 decoder by using two instances of the `en_dec_328` entity.

11. (15 points) Modify the following VHDL model to use block(s) instead of processes.

```
library ieee;
use ieee.std_logic_1164.all;

entity BUFF_REG is
  generic (STRB_DEL, EN_DEL, ODEL: TIME);
  port (DI: in std_logic_vector (1 to 8);
        DS1, NDS2, STRB : in std_logic;
        DO: out std_logic_vector (1 to 8));
end BUFF_REG;

architecture THREE_PROC of BUFF_REG is
  signal REG : std_logic_vector (1 to 8);
  signal ENBLD : std_logic;
begin
  PREG: process (STRB)
  begin
    if (STRB = '1') then
      REG <= DI after STRB_DEL;
    end if;
  end process PREG;

  ENABLE : process (DS1, NDS2)
  begin
    ENBLD <= DS1 and not NDS2 after EN_DEL;
  end process ENABLE;

  OUTPUT : process (REG, ENBLD)
  begin
    if (ENBLD = '1') then
      DO <= REG after ODEL;
    else
      DO <= "ZZZZZZZZ" after ODEL;
    end if;
  end process OUTPUT;
end THREE_PROC;
```

Consider the following VHDL code:

```
-----  
-- Entity declaration  
-----  
  
entity SCHED2 is  
    port (A, B, C, D, E, F: in INTEGER;  
          CLK : in BIT;  
          W, X, Y: out INTEGER);  
end SCHED2;  
  
-----  
-- Architecture declaration  
-----  
  
architecture HIGH_LEVEL of SCHED2 is  
    signal Z: INTEGER;  
begin  
    X <= (A - B) * Z;  
    Y <= (A * B) + Z;  
    Z <= (C * D) + D * (E + F);  
    W <= A/F + C*C + D* (A - B);  
end HIGH_LEVEL;
```

12. (14 points) The following tasks refer to the VHDL code above. Assume that there are no hardware constraints..

- a. (7 points) Derive an ASAP schedule.
- b. (7 points) Derive an ALAP schedule.

13. (10 points) Derive a list schedule using the critical path priority metric for the VHDL code above, using the following hardware constraint; all operations are done in an ALU module and there are two ALU modules available.

14. (1 point) _____ is one algorithmic-level synthesis task.

15. (1 point) _____ is the hardest problem.