CPE 426 Spring 2004 Midterm Solutions:

1.

```
package LOGIC_PKG is
  component AND2_OP
    port (A, B : in BIT; Z : out BIT);
  end component;
  component NAND2_OP
    port (A, B : in BIT; Z : out BIT);
  end component;
  component OR4_OP
    port (A, B, C, D : in BIT; Z : out BIT);
  end component;
end LOGIC_PKG;

use work.LOGIC_PKG.ALL;

entity EXPRESSION is
  port (A, B, C, D : in BIT;
        F : out BIT);
end EXPRESSION;

architecture STRUCTURAL of EXPRESSION is
  signal temp : bit_vector (0 to 7);
begin
  U1 : NAND2_OP port map (A, A, TEMP(0));
  U2 : NAND2_OP port map (B, B, TEMP(1));
  U3 : NAND2_OP port map (C, C, TEMP(2));
  U4 : AND2_OP port map (TEMP(0), TEMP(1), TEMP(2));
  U5 : AND2_OP port map (TEMP(2), C, TEMP(3));
  U6 : AND2_OP port map (TEMP(3), D, TEMP(4));
  U7 : AND2_OP port map (A, B, TEMP(5));
  U8 : AND2_OP port map (TEMP(5), C, TEMP(6));
  U9 : AND2_OP port map (TEMP(1), TEMP(2), TEMP(7));
  U10 : OR4_OP port map (TEMP(4), TEMP(6), TEMP(7), '0', F);
end STRUCTURAL;
```

2. A hardware description language is a high-level programming language with specialized constructs for modeling hardware.

3.

```
package MINE is
  function REVERSE(X : in bit_vector) return bit_vector;
end MINE;

package body MINE is
  function REVERSE(X : in bit_vector) return bit_vector is
    variable Y : bit_vector(X'range);
    variable low : integer;
    variable high : integer;
  begin
    if (X'left = X'low) then
      for i in 0 to X'length - 1 loop
        Y(X'low + X'length - i - 1) := X(i + X'low);
      end loop;
    else
```

```
      for i in 0 to X'length - 1 loop
        Y(X'low + i) := X(X'low + X'length - 1 - i);
      end loop;
    end if;
    return Y;
  end REVERSE;
end MINE;

use work.MINE.all;
entity TEST_REVERSE is
end TEST_REVERSE;

architecture TWISTED of TEST_REVERSE is
  signal A : bit_vector(5 downto 0) := "111000";
  signal B : bit_vector(24 to 35) := "000110001101";
  signal C : bit_vector(40 downto 34) := "1111110";
  signal D : bit_vector(40 downto 35);
  signal E : bit_vector(0 to 11);
  signal F : bit_vector(0 to 6);
begin
  process
  begin
    wait for 10 ns;
    D <= REVERSE(A);
    E <= REVERSE(B);
    F <= REVERSE(C);
    wait;
  end process;
end TWISTED;
```

4. Inertial delay is the delay which represents gate delay in VHDL.

5. All statements inside of a block are concurrent.

6. For the following function call, which function will be called? __A__

```
VARIABLE a, b : INTEGER;
b := decrement (a);
(a) FUNCTION decrement (x : INTEGER) RETURN INTEGER;
(b) FUNCTION decrement (x : REAL) RETURN REAL;
```

7. An array is an aggregate type in VHDL.

8.

```
entity GRAY2BCD is
  port (GRAY : in bit_vector(3 downto 0);
        BCD : out bit_vector(3 downto 0));
end GRAY2BCD;

architecture CONCURRENT of GRAY2BCD is
begin
  BCD <= "0000" when GRAY = "0000" else
         "0001" when GRAY = "0001" else
         "0010" when GRAY = "0011" else
         "0011" when GRAY = "0010" else
         "0100" when GRAY = "0110" else
         "0101" when GRAY = "1110" else
```

```
         "0110" when GRAY = "1010" else
         "0111" when GRAY = "1011" else
         "1000" when GRAY = "1001" else
         "1001" when GRAY = "1000"; --else
--         "1111";
end CONCURRENT;
```

9.

```
entity SMODEL is
  port
    (P1 : in BIT;
     P2 : out BIT;
     P3 : inout BIT);
end SMODEL;

architecture STRUCTURE of SMODEL is
  component UNIT
    port (C1, C2 : in BIT;
          C3 : out BIT);
  end component;
begin
  U1 : UNIT port map (C1 => P1, C2 => P3, C3=> P2);
end STRUCTURE;

architecture STRUCTURE_A of SMODEL is
  component UNIT
    port (C1, C2 : in BIT;
          C3 : out BIT);
  end component;
begin
  U2 : UNIT port map (C1 => P3, C2 => P1, C3=> P2);
end STRUCTURE_A;
```

10.

```
library ieee;
use ieee.std_logic_1164.all;

package TYPES is
  type MVL3 is ('Z', '0', '1');
  type SEASON_OF_YEAR is (SPRING, SUMMER, FALL, WINTER);
  type MONTH_NUMBER is range 1 to 12;
  type COST is range 0.0 to 1405.0;
  type HIGH_WORD is range 63 downto 32;
  type REG_32_HIGH is array HIGH_WORD of MVL3;
  type TABLE_3D is array (std_logic, std_logic, std_logic) of
std_logic;
end TYPES;
```

10. An entity X, when used in another entity, becomes a component in entity Y.

11. Boolean is an example of a built-in enumerated type.

12.

Present State	Next State sig_in='0'	Next State sig_in='1'	Output
a	a	d	1
b	b	c	0
c	d	a	1
d	e	b	0
e	b	c	0

This is a Moore machine, because the output depends only on the state.

13. Communication is the hardest problem.