

1. (5 points) Draw the transistor-level diagram of a CMOS inverter.
2. (10 points) Write a VHDL entity (3 points) and architecture (7 points) of a two-input AND gate with the generics, TIPDA and TIPDB, which reflect the delay on the routing to the inputs A and B, respectively of the AND gate.
3. (1 point) _____ models provide blanks for timing information that is provided by place and route tools.
4. (1 point) A(n) _____ is an integrated circuit produced for a specific application and produced in relatively small volumes.
5. (1 point) All sequential circuits should have a(n) _____ input.

6. (1 point) A(n) _____ is a primary design unit.

7. (5 points) If the NRE costs for FPGA and CBIC circuits are \$41,000 and \$237,000, respectively, and the cost of individual parts for FPGA and CBIC circuits are \$18 and \$5, respectively, what is the break-even manufacturing volume for these two types of circuits?

8. (5 points) What kind of hardware element will be inferred by a synthesis tool from the following model?

```
library ieee;
use ieee.std_logic_1164.all;

entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK, RESET : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;

architecture EXAMPLE of WIDGET is
begin
  process (CLK, RESET)
  begin
    if (RESET = '1') then
      Z <= '0';
    elsif (CLK = '1') then
      Z <= A nor B;
    end if;
  end process;
end EXAMPLE;
```

9. (1 point) _____ is a predefined enumerated type in VHDL.

10. (1 point) A(n) _____ is an example of a sequential VHDL statement.

11. (10 points) For the data lifetime chart shown, use the left edge algorithm to obtain an efficient register allocation.

	A	B	C	D	E	F	G	H	I	J	K	L
S1			X	X			X				X	
S2		X	X				X			X	X	
S3		X				X	X		X	X	X	
S4	X	X				X			X		X	X
S5	X					X		X	X		X	X
S6	X				X			X	X			X
S7					X				X			X

12. (6 points) (a) (4 points) Translate the following statement to an if-then-else statement:

```
transmit <= signal_a when state = idle else  
           signal_b when state = incoming else  
           signal_c when state = outgoing else  
           signal_d;
```

(b) (2 points) Can these two forms be used interchangeably? Why or why not?

13. (10 points) Build a 16-bit down counter with synchronous load and asynchronous reset. The outputs are three-state outputs, controlled by two separate signals – one for the lower 8 bits and one for the upper 8-bits. Inputs: clk, reset, load, data[15:0], upper_enable, lower_enable; output: count[15:0] (a) (3 points) entity (b) (7 points) architecture Include any necessary library or use statements.

14. (12 points) (a) (6 points) Write a single VHDL model which represents an exclusive-OR gate with an arbitrary number of inputs, N. (b) (6 points) Use that model as a component in an entity that represents a three input exclusive-OR gate with inputs a, b, c and output f

15. (6 points) Translate the following VHDL to two with-select-when statements:

```
case state is
  when idle => a <= "11"; b <= "00";
  when terminate | increase => a <= "01"; b <= "--";
  when maintain | decrease => a <= "10"; b <= "11";
  when others => a <= "11"; b <= "01";
end case;
```

Consider the following VHDL code:

```
-----  
-- Entity declaration  
-----  
  
entity SCHED2 is  
  port (A, B, C, D, E, F: in INTEGER;  
        CLK : in BIT;  
        W, X, Y: out INTEGER);  
end SCHED2;  
  
-----  
-- Architecture declaration  
-----  
  
architecture HIGH_LEVEL of SCHED2 is  
  signal Z: INTEGER;  
begin  
  X <= (A - B) * Z;  
  Y <= (A * B) + Z;  
  Z <= (C * D) + D * (E + F);  
  W <= A/F + C*C + D* (A - B);  
end HIGH_LEVEL;
```

16. (15 points) The following task refers to the VHDL code above. Assume that all operations are done in an ALU module and there are two ALU modules available. Derive a schedule for the operations using the freedom-directed algorithm.

17. (10 points) Model an arbiter in VHDL that is arbitrating between three devices. Device 1 has the highest priority while device 3 has the lowest priority. This arbiter controls access by various devices to a shared resource in a given system, such as a bus. Only one device can use the resource at a time. Assume that the active clock edge is the positive edge. Each device provides one input to the controller, called a request, and the controller produces a separate output for each device, called a grant. A device indicates its need to use the resource by asserting its request signal. Whenever the shared resource is not already in use, the controller considers all requests that are active. Based on a priority scheme, it selects one of the requesting devices and asserts its grant signal. When the device is finished using the resource, it deasserts its request signal. Make sure that there are no implied latches in your model.

