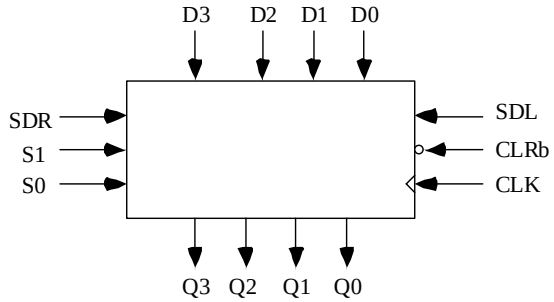
The University of Alabama in Huntsville
ECE Department
CPE 426 01
Midterm Exam
March 3, 2005

Name: _____

1. (10 points) A description of a 74194 4-bit bi-directional shift register follows: The CLRb input is asynchronous and active low and overrides all the other control inputs. All other state changes occur following the rising edge of the clock. If the control inputs S1 = S0 = 1, the register is loaded in parallel. If S1 = 1 and S0 = 0, the register is shifted right and SDR (serial data right) is shifted into Q3. IF S1 = 0 and S0 = 1, the register is shifted left and SDL is shifted into Q0. If S1 = S0 = 0, no action occurs.



Write a VHDL description of an 8-bit bi-directional shift register that uses two 74194s as components. The parallel inputs and outputs to the 8-bit register should be X and Y. The serial inputs should be RSD and LSD.

2. (1 point) VHDL is a strongly typed language. (True/False) _____

3. (15 points). Write a VHDL function that accepts a std_logic_vector of arbitrary length and an integer that specifies the number of bits the std_logic_vector is to be rotated to the left and returns the rotated std_logic_vector. Issue an error message if the integer is greater than the length of the input. For example:

Input: 0101111, 2
Output: 0111101

4. (1 point) A(n) _____ occurs when a signal changes value.

5. (1 point) All statements inside of a process are _____.

6. (3 points) For the following function call, which function will be called? _____

```
VARIABLE a, b : INTEGER;
b := decrement (a);

(a)          FUNCTION decrement (x : INTEGER) RETURN INTEGER;
(b)          FUNCTION decrement (x : REAL) RETURN REAL;
```

7. (1 point) A _____ binds an instantiated component to a library model

8. (15 points) Design an address decoder. One input to the address decoder is an 8-bit address, which can have any range with a length of 8, for example: std_logic_vector addr(8 to 15). The second input is check : std_logic_vector(5 down to 0). The address decoder will output Sel = ‘1’ if the upper 6 bits of the 8-bit address match the 6-bit check vector. For example, if addr = “10001010” and check = “1000--“ then Sel = ‘1’. Only the 6 leftmost bits of addr will be compared; the remaining bits are ignored. An ‘-‘ in the check vector is a don’t care.(a) (4 points) Write an entity for the device. (b) (11 points)Write an architecture for the device.

9. (6 points) Design a 2-to-1 multiplexer. (a) (2 points) Write a VHDL entity. (b) (4 points) Use concurrent signal assignments to implement the architecture.

10. (10 points)A DD flip-flop is similar to a D flip-flop, except that the flip-flop can change state (Q+ = D) on both the rising edge and falling edge of the clock input. The flip-flop has a direct reset input R, and R = 0 resets the flip-flop to Q = 0 independent of the clock. (a) (2 points) Write a VHDL entity for the DD flip-flop. (b) (6 points) Write a VHDL architecture for a DD flip-flop. (b) (2 points) Is this description synthesizable? Why or why not?

11. (15 points) For the following VHDL, assume that A changes to '1' at 5 ns. Give the values of A, B, C, D, E, and F each time a change occurs. Carry this out until no further change occurs. I

```
entity prob is
  port (D : inout bit);
end prob;

architecture PROB of PROB is
  signal A, B, C, E, F : bit;
begin
  P1: process (A, C)
  begin
    B <= A after 3 ns;
    E <= C after 5 ns;
  end process P1;
  C <= A after 10 ns;
  P2: process (C, E)
  begin
    F <= C and E after 4 ns;
  end process P2;
  D <= A or B or C or F after 1 ns;
end PROB;
```

Time	A	B	C	D	E	F
0 ns	0	0	0	0	0	0
5 ns	1	0	0	0	0	0

12. (21 points) Specify type declarations for the following data types.

a. (4 points) A four valued logic system, MVL4, with values ‘0’, ‘1’, ‘X’ and ‘Z’. Values ‘0’ and ‘1’ have the usual logic meaning and ‘X’ means unknown. Any uninitialized data item of this type should have value ‘X’.

b. (4 points) A GRADE_LEVEL enumeration data type.

c. (2 points) A data type AGE that can have integer values in the range from 1 to 120.

d. (2 points) A data type COST that can have real values between $0.00 and $1,405.00.

e. (2 points) A descending range data type HIGH_WORD with integer values from 63 to 32.

f. (3 points) A 64-bit ascending-index register composite data type, REG_64_HIGH, with index valued from the type HIGH_WORD declared above, and component values of type MVL4.

g. (4 points) A four-dimensional table, TABLE_4D, with index values and table entries all of type std_logic (which has been declared elsewhere and is visible).

13. (1 point) _____ is the hardest problem.