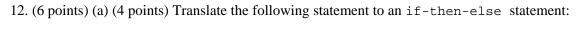
## The University of Alabama in Huntsville ECE Department CPE 526 01 Final Exam April 28, 2005

	Posting Code:
1. (5 points) Draw the transistor-level diag	ram of a CMOS inverter.
2. (10 points) Write a VHDL entity (3 po	ints) and architecture (7 points) of a two-input AND gate with h reflect the delay on the routing to the inputs A and B,
3. (1 point)by place and route tools.	models provide blanks for timing information that is provided
4. (1 point) A(n) and produced in relatively small volumes.	is an integrated circuit produced for a specific application
5. (1 point) All sequential circuits should h	nave a(n) input.

6. (1 point) A(n)	is a primary design unit.
	and CBIC circuits are \$41,000 and \$237,000, respectively, and CBIC circuits are \$18 and \$5, respectively, what is the breaktypes of circuits?
	ement will be inferred by a synthesis tool from the following
model?	
<pre>library ieee; use ieee.std_logic_1164.all;</pre>	;
entity WIDGET is  Port (A, B : in SIGNED (0  CLK, RESET : in std.  Z : out SIGNED(0 to  end WIDGET;	_logic;
architecture EXAMPLE of WIDO	GET is
<pre>process (CLK, RESET) begin   if (RESET = '1') then   Z &lt;= '0';</pre>	
<pre>elsif (CLK = '1') then    Z &lt;= A nor B; end if; end process;</pre>	
end EXAMPLE;	
9. (1 point ) is a pr	edefined enumerated type in VHDL.
10. (1 point) A(n)	is an example of a sequential VHDL statement.

11. (10 points) For the data lifetime chart shown, use the left edge algorithm to obtain an efficient register allocation.

	A	В	С	D	Е	F	G	Н	I	J	K	L
<b>S</b> 1			X	X			X				X	
S2		X	X				X			X	X	
<b>S</b> 3		X				X	X		X	X	X	
S4	X	X				X			X		X	X
S5	X					X		X	X		X	X
<b>S</b> 6	X				X			X	X			X
<b>S</b> 7					X				X			X



(b) (2 points) Can these two forms be used interchangeably? Why or why not?

13. (10 points) Build a 16-bit down counter with synchronous load and asynchronous reset. The outputs are three-state outputs, controlled by two separate signals – one for the lower 8 bits and one for the upper 8-bits. Inputs: clk, reset, load, data[15:0], upper\_enable, lower\_enable; output: count[15:0] (a) (3 points) entity (b) (7 points) architecture Include any necessary library or use statements.

14. (12 points) (a) (6 points) Write a single VHDL model which represents an exclusive-OR gate with an arbitrary number of inputs, N. (b) (6 points) Use that model as a component in an entity that represents a three input exclusive-OR gate with inputs a, b, c and output f

15. (6 points) Translate the following VHDL to two with-select-when statements:

```
case state is
  when idle => a <= "11"; b <= "00";
  when terminate | increase => a <= "01"; b <= "--";
  when maintain | decrease => a <= "10"; b <= "11";
  when others => a <= "11"; b <= "01";
end case;</pre>
```

## Consider the following VHDL code:

```
-- Entity declaration
entity SCHED2 is
 port (A, B, C, D, E, F: in INTEGER;
       CLK : in BIT;
       W, X, Y: out INTEGER);
end SCHED2;
-- Architecture declaration
______
architecture HIGH_LEVEL of SCHED2 is
 signal Z: INTEGER;
begin
 X <= (A - B) * Z;
 Y \le (A * B) + Z;
 Z \ll (C * D) + D * (E + F);
 W \ll A/F + C*C + D*(A - B);
end HIGH_LEVEL;
```

16. (15 points) The following task refers to the VHDL code above. Assume that all operations are done in an ALU module and there are two ALU modules available. Derive a schedule for the operations using the freedom-directed algorithm.

17. (10 points) Model an arbiter in VHDL that is arbitrating between three devices. Device 1 has the highest priority while device 3 has the lowest priority. This arbiter controls access by various devices to a shared resource in a given system, such as a bus. Only one device can use the resource at a time. Assume that the active clock edge is the positive edge. Each device provides one input to the controller, called a request, and the controller produces a separate output for each device, called a grant. A device indicates its need to use the resource by asserting its request signal. Whenever the shared resource is not already in use, the controller considers all requests that are active. Based on a priority scheme, it selects one of the requesting devices and asserts its grant signal. When the device is finished using the resource, it deasserts its request signal. Make sure that there are no implied latches in your model.

