The University of Alabama in Huntsville
ECE Department
CPE 526 01
Final Exam
April 27, 2009

Name: _____

1. (5 points) Draw the transistor-level diagram of a CMOS inverter.

2. (5 points) Consider the following structural VHDL model.

```
entity SMODEL is
   port
     (P1 : in BIT;
      P2 : out BIT;
      P3 : inout BIT);
end SMODEL;

architecture STRUCTURE of SMODEL is
   component UNIT
      port (C1, C2, : in BIT; C3 : out BIT);
   end component;

begin
  U1 : UNIT port map (C1 => ?, C2 => ?, C3 => ?);
end STRUCTURE;
```

   (a) (3 points) Complete the structural description by giving a legal set of port-to-port connections for entity ports P1, P2, and P3 and component ports C1, C2, and C3.
   (b) (2 points) Is there more than one possible set of legal port-to-port connections?

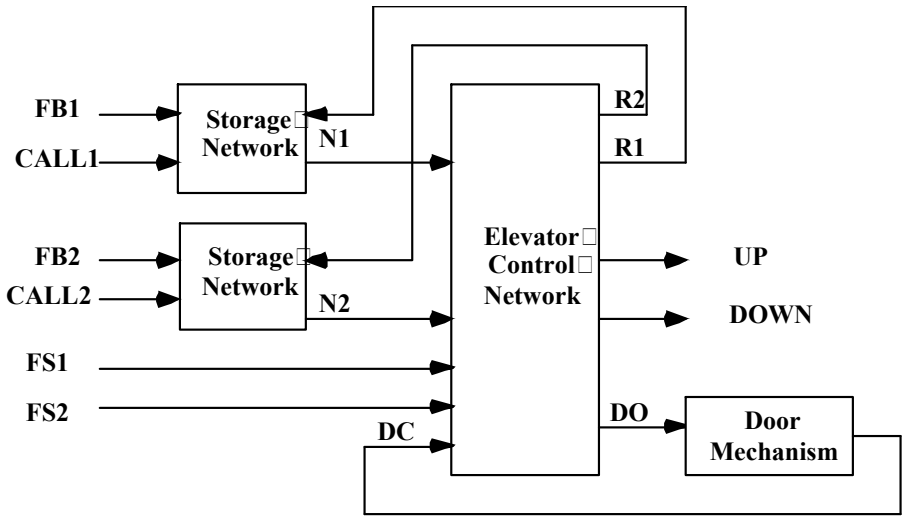
3. (10 points) For the following VHDL architecture, give the values of A, B, C, D, E, and F each time a change occurs. Carry this out until no further change occurs. I

```
entity prob is
  port (D : inout bit);
end prob;

architecture PROB of PROB is
  signal A, B, C, E, F : bit;
begin
  P1: process (A, C)
  begin
    B <= A after 3 ns;
    E <= C after 5 ns;
  end process P1;
  C <= A after 10 ns;
  P2: process (C, E)
  begin
    F <= C and E after 4 ns;
  end process P2;
  D <= A or B or C or F after 1 ns;
  process
    A <= '1' after 5 ns;
    wait;
  end process'
end PROB;
```

Time	A	B	C	D	E	F
0 ns	0	0	0	0	0	0

4. (15 points) The block diagram for an elevator controller for a building with two floors is shown below. The inputs FB1 and FB2 are floor buttons in the elevator. The inputs CALL1 and CALL2 are call buttons in the hall. The inputs FS1 and FS2 are floor switches that output a 1 when the elevator is at the first or second floor landing. Outputs UP and DOWN control the motor, and the elevator is stopped when UP = DOWN = 0. N1 and N2 are flip-flops that indicate when the elevator is needed on the first or second floor. R1 and R2 are signals that reset these flip-flops. DO = 1 causes the door to open, and DC = 1 indicates that the door is closed. (a) Write a VHDL entity for the controller. (b) Write a VHDL architecture that models the functionality of the controller.



5. (5 points) If the NRE costs for FPGA and ASIC circuits are $30,000 and $750,000, respectively, and the cost of individual parts for FPGA and ASIC circuits are $30 and $5, respectively, what is the break-even manufacturing volume for these two types of circuits?

6. (10 points) Write a VHDL procedure that will add two n x m matrices of integers, C <= A + B. The procedure call should be of the form addM(A, B, C). The procedure should report an error if the number of rows in A and B are not the same or if the columns in A and B are not the same. Make no assumptions about the high and low values or direction of the ranges for either dimensions.

7. (5 points) Rewrite the following VHDL to use processes instead of blocks. The processes should have the exact same behavior as the blocks.

```
use WORK.TSL.all,WORK.SYS.all;
entity I8212 is
 generic (GDEL,FFDEL,BUFDEL: TIME);
 port (DI: in WORD;
       DO: out WORD;
       NDS1,DS2,MD,STB,NCLR: in BIT;
       NINT: out BIT := '1');
end I8212;

architecture BEHAVIOR of I8212 is
begin
I8212_BLK: block

signal S0,S1,S2,S3,S4: BIT;
signal SRQ: BIT;
signal Q: WORD;
begin

INT_BLK:
block (S1='1' and S4='1')
begin
 Q <= guarded DI after FFDEL;
 Q <="00000000" after FFDEL when (S1='0' and S4='0') else
      Q;
 DO <= Q after BUFDEL when (S3 = '1') else
      "ZZZZZZZZ" after BUFDEL;
end block INT_BLK;

S0 <= not NDS1 and DS2 after GDEL;
S1 <= (S0 and MD) or (STB and not MD) after (2*GDEL);
S2 <= (S0 nor (not S4)) after GDEL;
S3 <= (S0 or MD) after GDEL;
S4 <= (S1 OR NCLR) after GDEL;
SRQ <= '1' after FFDEL when (S2= '0') else
       '0' after FFDEL when (S2= '1') and (not STB'STABLE) and (STB='0') else
        SRQ;
NINT <= not SRQ nor S0 after GDEL;
end block I8212_BLK;
end BEHAVIOR;
```

8. (10 points) Create a VHDL entity named `en_dec_328` that represents a 3-to-8 decoder with an active-low enable input which has an architecture which uses a case statement to represent the functionality of the decoder. Create a second entity and its accompanying architecture that represents a 4-to-16 decoder by using two instances of the `en_dec_328` entity.

9. (2 points)_____ measures the progress of all tests in fulfilling the verification plan requirements

10. (2 points) An _____ is a construct that represents a bundle of wires but also has intelligence such as synchronization and functional code. _____ allow a module to easily tap a subset of signals from an _____(same as first blank) and can be used to check signal direction.

11. (4 points) A constrained random test (CRT) is made of two parts
    a. _____
    b. _____

12. (8 points) (a) (5 points) Write a single VHDL model which represents an AND gate with an arbitrary number of inputs, N. (b) (3 points) Use that model as a component in an entity that represents a four input AND gate with inputs a, b, c, d and output f

13. (5 points) What kind of hardware element will be inferred by a synthesis tool from the following model?

```
library ieee;
use ieee.std_logic_1164.all;

entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK, RESET : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;

architecture EXAMPLE of WIDGET is
begin
  process (CLK, RESET)
  begin
    if (RESET = '1') then
      Z <= '0';
    elsif (CLK = '1') then
        Z <= A nor B;
    end if;
  end process;
end EXAMPLE;
```

14. (2 points) _____(True or False)The SystemVerilog standard specifies the meaning of constraint expressions, the legal values that are created, and the precise order in which the solver should operate.

15. (2 points) Which of the following are true? _____ Multiple choice

a. Constraints execute from top to bottom.
b. Constraints are bidirectional, meaning that the constraints on all random variables are solved concurrently.
c. both a and b
d. neither a nor b

16. (10 points) Modify the following VHDL model by adding a parameter that sets the number of flip-flops in the counter. Also, add an input which is loaded with an asynchronous load input signal which is active low.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity UPCOUNT is
  port ( CLOCK, RESETN, E : in std_logic;
         Q                : out std_logic_vector (3 downto 0));
end UPCOUNT;

architecture BEHAVIOR of UPCOUNT is
  signal COUNT : std_logic_vector (3 downto 0);
begin
  process (CLOCK, RESETN)
  begin
    if RESETN = ‘0’ then
      COUNT <= “0000”;
    elsif (CLOCK’event and CLOCK = ‘1’) then
      if E = ‘1’ then
        COUNT <= COUNT + 1;
      else
         COUNT <= COUNT;
      end if;
  end process
  Q <= COUNT;
```