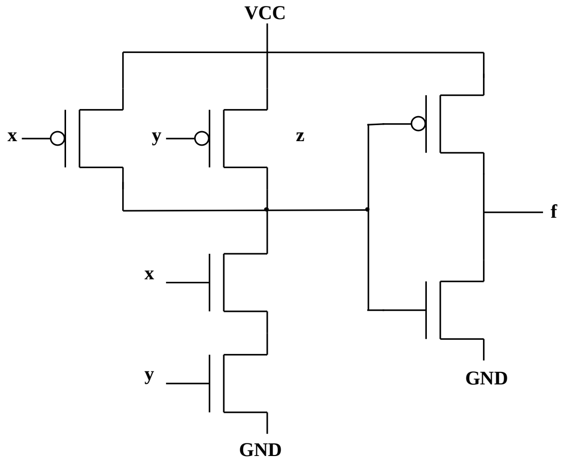
The University of Alabama in Huntsville
ECE Department
CPE 426 01
Final Exam Solution
Spring 2010

1. (6 points) Draw the transistor-level diagram of a CMOS AND gate.



2. (6 points) What is wrong with the following model of a 4-to-1 MUX? (It is not a syntax error.)

For this model to work correctly, `sel` needs to be a variable.

```
architecture mux_behavioral of 4to1mux is
signal sel: integer range 0 to 3;
begin
  process(A, B, I0, I1, I2, I3)
  begin
   sel <= 0;
    if A = '1' then
      sel <= sel + 1;
    end if
    if B = '1' then
      sel <= sel + 2;
    end if;
    case sel is
      when 0 => F <= I0;
      when 1 => F <= I1;
      when 2 => F <= I2;
      when 3 => F <= I3;
    end case;
  end process
end mux_behavioral;
```

3. (18 points) A synchronous sequential circuit has one input and one output plus a synchronous reset which is active low. If the input sequence 1001 or 0101 occurs, an output of two successive 1s will occur. The first of these 1s should occur coincident with the last input of the 1001 or 0101 sequence. The network should reset when the second 1 output occurs. For example,

   Input sequence: 01101100010010 1101010
   Output sequence: 00000000000011 0000011

   a) (4 points) Write a VHDL entity for this circuit.
   b) (14 points) Write a VHDL architecture for this circuit.

```
   library ieee;
   use ieee.std_logic_1164.all;

   entity sequence is
     port (X : in std_logic;
           RESET : in std_logic;
           Z : out std_logic;
           CLK : in std_logic);
   end sequence;

   architecture behav of sequence is
     --signal window : std_logic_vector(3 downto 0);
     type state_type is (INIT, SAMPLE, EXTRA_ONE);
     signal STATE : state_type;
   begin
     process(CLK)
       variable window : std_logic_vector(3 downto 0);
     begin
       if (RESET = '1') then
         STATE <= INIT;
         Z <= '0';
       elsif (CLK'event and CLK = '1') then
         case STATE is
           when SAMPLE =>
             window := window(2 downto 0) & X;
             if (window = "1001" or window = "0101") then
               STATE <= EXTRA_ONE;
               Z <= '1';
             else
               STATE <= SAMPLE;
               Z <= '0';
             end if;
           when EXTRA_ONE =>
             window := "0000";
             STATE <= SAMPLE;
             Z <= '1';
           when INIT =>
             window := "0000";
             STATE <= SAMPLE;
             Z <= '0';
         end case;
       end if;
     end process;
end behav;
```

4. (4 points) List the four types of paths that must be considered when doing timing analysis of sequential circuits.

inputs to outputs

inputs to inputs of memory elements

outputs of memory elements to inputs of memory elements

outputs of memory elements to outputs

5. (1 point) **_Standard cells_** are primitives that are all the same height and varying widths.

6. (10 points) A synchronous (4-bit) up/down decade counter with outputs COUNT and CO works as follows: All state changes occur on the rising edge of the CLK input, except the asynchronous clear (CLR). When CLR = 0, the counter is reset regardless of the values of the other inputs. The inputs are DATA, CLR, LOAD, EN, UP.

If the LOAD input is 0, the data input D is loaded into the counter.
If LOAD = EN = UP =1, the counter is incremented.
If LOAD = EN =1, and UP = 0, the counter is decremented.
If LOAD = EN = UP = 1, the carry output (CO) =1 when the counter is in state 9.
If LOAD = EN = 1 and UP = 0, the carry output (CO) =1 when the counter is in state 0.

Create a SystemVerilog interface for this circuit that has a clocking block that defines directions relative to the test bench.

```
interface counter_if(input bit clk);
  logic [3:0] COUNT;
  logic CO, LOAD, EN, UP;
  logic [3:0] D;

  clocking cb @(posedge clk);
    output LOAD, D, EN, UP;
    input COUNT, CO;
  endclocking

  modport TEST (clocking cb);
endinterface
```

7. (20 points) a) (15 points) Write a VHDL model of a D flip-flop which has asynchronous Preset and Clear and which is negative edge triggered. Your model should have 6 generics, with default values of 5 ns, as listed in the table below. (Clear has priority over Reset)
b) (5 points) Create an instantiation of the flip-flop which has the following timing specifications.

Parameter	From Input	To Output	Specification
TPLH	Preset	Q	16 ns
TPHL	Preset	Q	25 ns
TPLH	Clear	Q	13 ns
TPHL	Clear	Q	22 ns
TPLH	Clock	Q or Q’	11 ns
TPHL	Clock	Q or Q’	20 ns

```
library ieee;
use ieee.std_logic_1164.all;

entity dff_generic is
  generic (TPLH_PQ, TPHL_PQ,
           TPLH_CQ, TPHL_CQ,
           TPLH_CKQ, TPHL_CKQ : time := 5 ns);
  port (D, CLK, CLEAR, PRESET : in std_logic;
        Q, QN : out std_logic);
end dff_generic;

architecture behav of dff_generic is
begin
  process (CLEAR, PRESET, CLK)
    variable QLAST, QTEMP : std_logic;
  begin
    QLAST := QTEMP;
    if (CLEAR'event) then
      if (CLEAR = '1') then
        QTEMP := '0';
      else
        QTEMP := '1';
      end if;
    elsif (PRESET'event) then
      if (PRESET = '1') then
        QTEMP := '1';
      else
        QTEMP := '0';
      end if;
    elsif (CLK'event and CLK = '0') then
      if (D = '1') then
        QTEMP := '1';
      elsif (D = '0') then
        QTEMP := '0';
      end if;
    end if;
    if (CLEAR'event) then
      if (QTEMP = '1' and QLAST = '0') then
        Q <= QTEMP after TPLH_CQ;
        QN <= not QTEMP after TPHL_CQ;
      elsif (QTEMP = '0' and QLAST = '1') then
        Q <= QTEMP after TPHL_CQ;
        QN <= not QTEMP after TPLH_CQ;
      end if;
    elsif (PRESET'event) then
      if (QTEMP = '1' and QLAST = '0') then
        Q <= QTEMP after TPLH_PQ;
        QN <= not QTEMP after TPHL_PQ;
      elsif (QTEMP = '0' and QLAST = '1') then
        Q <= QTEMP after TPHL_PQ;
        QN <= not QTEMP after TPLH_PQ;
      end if;
      elsif (CLK'event and CLK = '0') then
        if (QTEMP = '1' and QLAST = '0') then
          Q <= QTEMP after TPLH_CKQ;
          QN <= not QTEMP after TPHL_CKQ;
        elsif (QTEMP = '0' and QLAST = '1') then
          Q <= QTEMP after TPHL_CKQ;
          QN <= not QTEMP after TPLH_CKQ;
        end if;
      end if;
    end process;
  end behav;
```

8. (5 points) If the NRE costs for FPGA and ASIC circuits are $35,000 and $1,500,000, respectively, and the cost of individual parts for FPGA and ASIC circuits are $45 and $7, respectively, what is the break-even manufacturing volume for these two types of circuits?

   35,000 +45x = 1,500,000 +7x, 38x = 1,465,000, x = 38,553

9. (12 points) Write a procedure that accepts a `std_logic_vector` of arbitrary length and returns integers which represent the total number of ‘1’s, the total number of ‘0’s and the total number of ‘Z’s contained in the `std_logic_vector`.

```
library ieee;
use ieee.std_logic_1164.all;

package needit is
  procedure count_them (x : in std_logic_vector;
                        num_ones, num_zeros, num_zs : out integer);
end needit;

package body needit is
  procedure count_them (x : in std_logic_vector;
                        num_ones, num_zeros, num_zs : out integer) is
    variable n_ones, n_zeros, n_zs : integer;
  begin
    n_ones := 0;
    n_zeros := 0;
    n_zs := 0;
    for i in x'range loop
      if (x(i) = '1') then
        n_ones := n_ones + 1;
      elsif (x(i) = '0') then
        n_zeros := n_zeros + 1;
      elsif (x(i) = 'Z') then
        n_zs := n_zs + 1;
      end if;
    end loop;
    num_ones := n_ones;
    num_zeros := n_zeros;
    num_zs := n_zs;
  end count_them;
end needit;
```

10. (2 points) A _ **cover group** _ is similar to a class and contains cover points, options, formal arguments, and an optional trigger.

11. (2 points) _ **True** _ True or False? Having both designer and verifier create independent interpretations of the specification provides reduncancy.

12. (4 points) _ **Path** _ and _ **line** _ are two types of code coverage.

13. (6 points) What kind of hardware element will be inferred by a synthesis tool from the following model?

```
library ieee;
use ieee.std_logic_1164.all;

entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK, RESET : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;

architecture EXAMPLE of WIDGET is
begin
  process (CLK, RESET)
  begin
    if (CLK = ‘1’ and CLK’EVENT) then
      if (RESET = ‘1’) then
        Z <= ‘0’;
      else
        Z <= A nor B;
      end if;
    end if;
  end process;
end EXAMPLE;
```

A flip-flop with synchronous reset.

14. (2 points) _ **False** _(True or False) The SystemVerilog standard specifies the meaning of constraint expressions, the legal values that are created, and the precise order in which the solver should operate.

15. (2 points) Which of the following are true? _ **d** _ Multiple choice

- a. Verification starts with interpretation of the specification.
- b. All testbenches share some common structure of stimulus generation and response checking.

c. The testbench simulates the design under test.
d. a and b
e. a, b and c