The University of Alabama in Huntsville
ECE Department
CPE 426 01
Final Exam
May 1, 2014

Name: _____

1. (6 points) Draw the transistor-level diagram of a CMOS inverter.

2. (5 points) If the NRE costs for CBIC and ASIC circuits are $400,000 and $2,500,000, respectively, and the cost of individual parts for CBIC and ASIC circuits are $35 and $11, respectively, what is the break-even manufacturing volume for these two types of circuits?

3. (1 point) The starting point from which a verification plan can be created is a

_____.

4 (1 point) List one type of coverage considered during the verification process.

_____.

5. (8 points) For the process given below, A, B, C, and D are all integers that have a value of 0 at time = 10 ns. If E changes from '0' to '1' at time 20 ns, specify all resulting changes. Indicate the time at which each change will occur, the signal/variable affected, and the value to which it will change.

```
process
  variable F : integer := 1; variable A : integer := 0;
begin
  wait on E;
  A := 1;
  F := A + 5;
  B <= F + 1 after 5 ns;
  C <= B + 2 after 10 ns;
  D <= C + 5 after 15 ns;
  A := A + 5;
end process;
```

Scheduling Rules	Transport	Inertial
New before existing	Overwrite existing	Overwrite existing
New after existing	Append new	If $v_{new} = v_{existing}$, append new Elsif t_{new}-$t_{existing}$ > reject append new Else overwrite existing

6. (2 points) List two layers that may be present in a layered testbench:

_____

_____

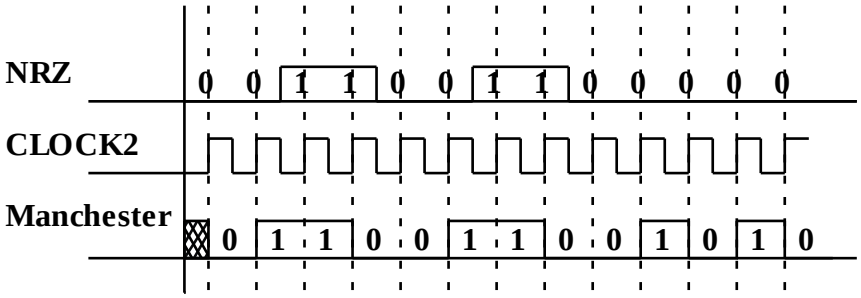
7. (1 point) A(n) _____ is a construct in System Verilog that represents a bundle of wires and has intelligence.

8. (10 points) Write a VHDL function that converts a 5-bit std_logic_vector to an integer. If any of the values are not '0' are '1', report an error. Note that the integer value of the binary number $a_4a_3a_2a_1a_0$ can be computed as $((((0 + a_4)*2 + a_3)*2 + a_2)*2 + a_1)*2 + a_0$

9. (1 point) A(n) _____ is an integrated circuit produced for a specific application and produced in relatively small volumes.

10. (1 point) _____ are inserted into VHDL models to give instructions to synthesis or other tools.

11. (15 points) Design a Moore state machine in VHDL which converts NRZ (non-return-to-zero) coding to Manchester coding. In NRZ coding, each bit is transmitted for one bit time without any change. For the Manchester code, a 0 is transmitted as 0 for the first half of the bit time and 1 for the second half, but a 1 is transmitted as 1 for the first half and 0 for the second half. In order to do this conversion, use a clock(CLOCK2) that is twice the frequency of the basic clock. Note that if the NRZ bit is 0, it will be 0 for two CLOCK2 periods. Similarly, if the NRZ bit is 1, it will be 1 for two CLOCK2 periods. Your design should have an active low synchronous reset and work with CLOCK2.



12. (6 points) In the following VHDL, `state` and `nextstate` are integers with a range of 0 to 2.

```
process (state, X)
begin
  case state is
    when 0=> if X = '1' then nextstate <= 1;
    when 1 => if X = '0' then nextstate <= 2;
    when 3 => If X = '1' then nextstate <= 0;
  end case
end process;
```

a. Explain why a latch would be created when the code is synthesized.
b. Make changes in the code that would eliminate the latch.

13. (12 points) (a) Write a VHDL entity and architecture for a circuit that has four inputs and three outputs. The 3-bit output should be a binary number equal to the number of 1's found in the inputs. (b) Write a VHDL entity and architecture for a circuit that counts the number of 1's in a 12-bit number. Use three of the modules from (a) along with overloaded addition operators.

14. (1 point) The @ construct in System Verilog is similar to the _____ construct in VHDL.

15. (1 point) A _____ test environment allows you to run hundreds of tests without having to hand check the results.

16. (12 points) Create a class `Test_problem` containing two random variables, 8-bit `data` and 4-bit `address`. Create a constraint block so that:
    a. `data` is always equal to 5
    b. The probability of `address == 0` is 10%
    c. The probability of `address` being between [1:14] is 80%
    d. The probability of `address == 15` is 10%

    In an initial block, construct a `Test_problem` object and randomize it.

17. (1 point) _____ is an example of an unconstrained array.

18. (1 point) _____ is an annoyingly strongly typed language.

19. (12 points) Design an interface and testbench for the ARM Advanced High-performance Bus (AHB). You are provided a bus master as verification IP that can initiate AHB transactions. You are testing a slave design. The testbench instantiates the interface, slave, and master. Your interface will display an error if the transaction type is not IDLE or NONSEQ on the negative edge of HCLK. The AHB signals are described below.

Signal	Width	Direction	Description
HCLK	1	Output	Clock
HADDR	21	Output	Address
HWRITE	1	Output	Write flag: 1=write, 0=read
HTRANS	2	Output	Transaction type: 2'b00=IDLE, 2'b10=NONSEQ
HWDATA	8	Output	Write data
HRDATA	8	Input	Read data

20. (3 points)) The three primary types of design units are _____,

_____, and _____