The University of Alabama in Huntsville
ECE Department
CPE 526 01
Midterm Exam
March 6, 2014

Name: _____

1. (15 points) Write a function, weaken, that maps a standard-logic value to the same value, but with weak drive strength. Thus, '0' and 'L' are mapped to 'L', '1' and 'H' are mapped to 'H', 'X' and 'W' are mapped to 'W' and all other values are unchanged.

2. (8 points) Write the equivalent process for the conditional signal assignment statement

```
with bit_vector'(s, r) select
  Q <= unaffected when "00",
       '0' when "01",
       '1' when "10" | "11";
```

3. (1 point) _____ delay is the delay which represents gate delay in VHDL
4. (1 point) A process is triggered whenever an event occurs on a signal that is in the _____ of the process.
5. (1 point) In order to specify edge behavior the _____ attribute is used in concurrent statements.
6. (1 point) _____(True or False) A D flip-flop and a D latch have the same behavior.
7. (1 point) _____ (True or False) It is possible to make aggregate assignments in VHDL.

8. (15 points) A 4-bit magnitude comparator chip compares two unsigned 4-bit numbers A and B and produces outputs to indicate whether A < B, A = B, or A > B. There are three output signals to indicate each of the above conditions. Note that exactly one of the output lines will be high and the other two lines will be low at any time. Write a behavioral VHDL model for the 4-bit comparator.

```
entity COMPARE is
  port (A : in bit_vector (3 downto 0);
        B : in bit_vector (3 downto 0);
        LT, EQ, GT : out bit);
end entity COMPARE;
```

9. (17 points) Develop a VHDL model of a 14-bit counter with parallel load inputs using instances of the 4-bit counter whose entity is given. Ensure that any unused inputs are properly connected to a constant driving value.

```
entity COUNTER is
  port (CLK_N, LOAD_EN : in std_ulogic;
        D : in std_ulogic_vector (3 downto 0);
        Q : out std_ulogic_vector (3 downto 0));
end entity COUNTER;
```

10. (20 points) Given the following VHDL, indicate all transactions and events. Give the values of A, B, C, D, E, and F each time a change occurs. Carry this out until no further change occurs.

```
entity PROB is
  port (D : inout bit);
end PROB;
architecture PROB of PROB is
  signal A, B, C, E, F : bit;
begin
  process
    A <= '1' after 5 ns, '0' after 12
ns;
    wait;
  end process;
  P1: process (A, C)
  begin
    B <= A after 2 ns;
    E <= C after 7 ns;
  end process P1;
  C1: C <= transport A and B after 6
ns;
  P2: process (C, E)
  begin
    F <= reject 3 ns inertial C and E
         after 5 ns;
  end process P2;
  C2: D <= A or B or C or F after 2 ns;
end PROB;
```

Time	A	B	C	D	E	F
0 ns	0	0	0	0	0	0
5 ns	1	0	0	0	0	0

Time Event Processes Triggered Scheduled Transactions Event?

Scheduling Rules	Transport	Inertial
New before existing	Overwrite existing	Overwrite existing
New after existing	Append new	If $v_{new} = v_{existing}$, append new Elsif $t_{new}-t_{existing} >$ reject append new Else overwrite existing

11. (10 points) Draw the state diagram for the following state machine. Is it a Moore machine or a Mealy machine?

```
entity STATE_MACHINE is
  port (SIG_IN ; in bit; CLK, RST : in bit;
        SIG_OUT : out bit);
end STATE_MACHINE;

architecture STATE_MACHINE of STATE_MACHINE is
  type STATE_TYPE is (A, B, C, D, E);
  signal CURRENT_STATE, NEXT_STATE : STATE_TYPE;
begin
  process (SIG_IN, CURRENT_STATE)
  begin
    SIG_OUT <= '0';
    NEXT_STATE <= C;
    case CURRENT_STATE
      when A =>
        if SIG_IN = '0' then
          NEXT_STATE <= C;
          SIG_OUT <= '1';
        else
          NEXT_STATE <= D;
        end if;
      when B =>
        if SIG_IN = '0' then
          NEXT_STATE <= B;
        else
          NEXT_STATE <= C;
        end if;
          SIG_OUT <= '1';
      when C =>
        if SIG_IN = '1' then
          SIG_OUT <= '1';
          NEXT_STATE <= A;
        else
          NEXT_STATE <= B;
        end if;
          SIG_OUT <= '1';
      when D =>
        if SIG_IN = '0' then
          NEXT_STATE <= E;
        end if;
      when E =>
        if SIG_IN = '1' then
          NEXT_STATE <= C;
        end if;
    end case;
  end process;
  process (CLK)
  begin
    if (RST = '0') THEN
      CURRENT_STATE <= A;
    elsif (CLK'event and CLK = '1') then
      CURRENT_STATE <= NEXT_STATE;
    end if;
  end process;
end STATE_MACHINE;
```

12. (10 points) Write a VHDL description for a rising edge D-type edge-triggered flip-flop with synchronous set and reset inputs active high and two outputs. Label the data, clock, set and reset inputs, d, c, s, and r, respectively. s and r cannot simultaneously be active.
    a. (3 points) Write an entity.
    b. (7 points) Write a synthesizable behavioral architecture.