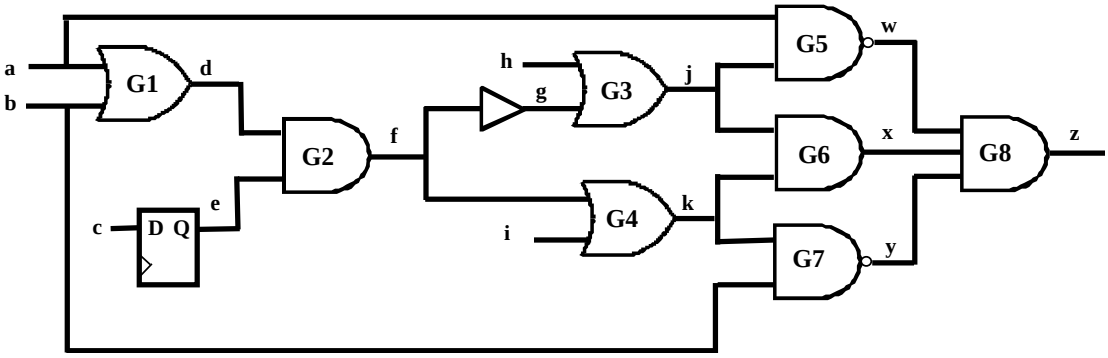
The University of Alabama in Huntsville
ECE Department
CPE 628 01
Final Exam Solution
Fall 2008

1. (10 points) Using the circuit shown and the D-algorithm, compute the vector that can detect the fault f/0. Note that even though the circuit is sequential, it can be viewed as a combinational circuit because the D flip-flop does not have an explicit feedback.



a	b	d	e	f	g	h	i	j	k	w	x	y	z	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	First, excite the fault.
		1	1	D										
X	X	1	1	D	X	X	X	X	X	X	X	X	X	
				D	D									
X	X	1	1	D	D	X	X	X	X	X	X	X	X	D frontier – G3, G4, pick G3
					D	0		D						
X	X	1	1	D	D	0	X	D	X	X	X	X	X	D frontier – G4, G5, G6, pick G5
1								D		D’				
1	X	1	1	D	D	0	X	D	X	D’	X	X	X	D frontier – G4, G6, G8, pick G8
										D’	1	1	D’	
1	X	1	1	D	D	0	X	D	X	D’	1	1	D’	J frontier – G6, G7, pick G6
								1	1		1			
1	X	1	1	D	D	0	X	C	1	D’	1	1	D’	Go back to before picked G8
1	X	1	1	D	D	0	X	D	X	D’	X	X	X	Pick G6
								D	1		D			
1	X	1	1	D	D	0	X	D	1	D’	D	X	X	No path, go back and pick G4
1	X	1	1	D	D	0	X	D	X	D’	X	X	X	
				D			0		D					
1	X	1	1	D	D	0	0	D	D	D’	X	X	X	
								D	D		D			
1	X	1	1	D	D	0	0	D	D	D’	D	X	X	No path, go back to G3, G4, pick G4
X	X	1	1	D	D	X	X	X	X	X	X	X	X	
				D			0		D					
X	X	1	1	D	D	X	X	X	D	X	X	X	X	D frontier G6, G7, pick G6
								1	D		D			
X	X	1	1	D	D	X	X	1	D	X	D	X	X	D frontier, G7, G8, pick G8
										1	D	1	D	
X	X	1	1	D	D	X	X	1	D	1	D	1	D	J frontier, G5, G7, pick G5
0								1		1				
0	X	1	1	D	D	X	X	1	D	1	D	1	D	J frontier G7
	0								D			1		
0	0	1	1	D	D	X	X	1	D	1	D	1	D	Implications on G1
0	0	0												
0	0	C	1	D	D	X	X	1	D	1	D	1	D	Conflict, no other paths, untestable

2. (1 point) _EXTEST, SAMPLE, PRELOAD, BYPASS_ is a mandatory instruction for standard 1149.1.

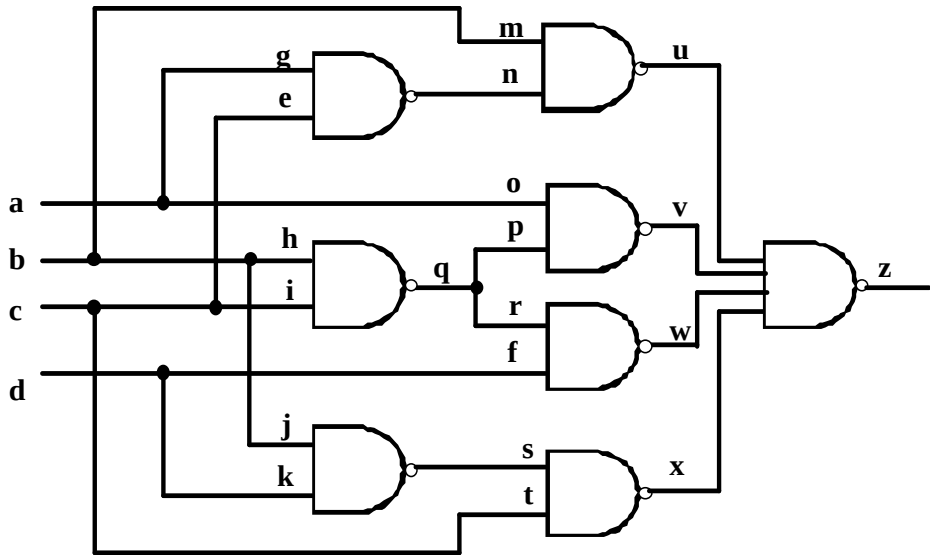
3. (1 point) The _Test Access Port Controller_ is a 16-state finite-state machine that controls circuit operation in standard1149.1.

4. (1 point) _Apply_ is a derived event in 1500.

5. (1 point) 1149.6 is like 1149.1 except that it allows for _analog signaling, AC coupling, high speed_.

6. (1 point) The most important feature of the 1500 standard is the provision of a _wrapper_ on the boundary (I/O) terminals of each core.

7. (10 points) For the circuit shown and the two faults α = u/0, β = a/1, use the parallel-pattern single-fault propagation technique to identify which faults can be detected by the test patterns
(a, b, c, d) = (0, 1, 1, 1), (0, 1, 1, 0), (0, 0, 1, 0}.



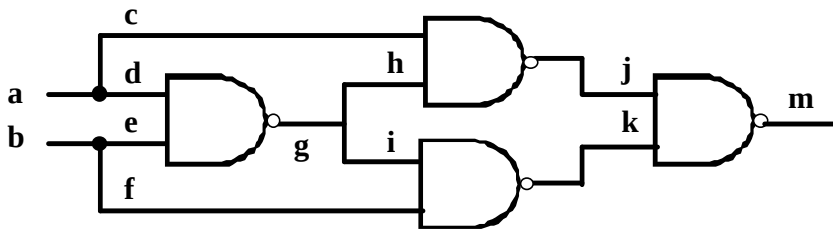
Fault-free	a	b	c	d	e	f	g	h	i	j	k	m	n	o	p	q	r	s	t	u	v	w	x	z
P1	0	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1
P2	0	1	1	0	1	0	0	1	1	1	0	1	1	0	0	0	0	1	1	0	1	1	0	1
P3	0	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	0	1

α	a	b	c	d	e	f	g	h	i	j	k	m	n	o	p	q	r	s	t	u	v	w	x	z
P1	0	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1
P2	0	1	1	0	1	0	0	1	1	1	0	1	1	0	0	0	0	1	1	0	1	1	0	1
P3	0	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	0	1

β	a	b	c	d	e	f	g	h	i	j	k	m	n	o	p	q	r	s	t	u	v	w	x	z
P1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	**0**
P2	1	1	1	0	1	0	1	1	1	1	0	1	0	1	0	0	0	1	1	1	1	1	0	1
P3	1	0	1	0	1	0	1	0	1	0	0	0	0	1	1	1	1	1	1	1	0	1	0	1

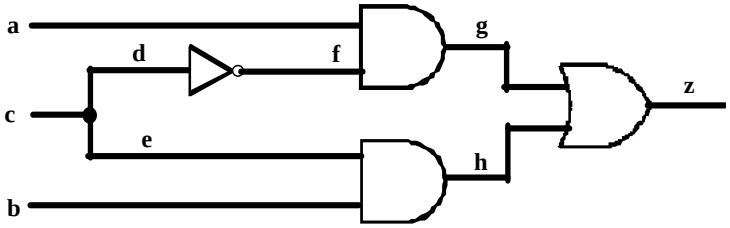
The pattern (a, b, c, d) = (0, 1, 1, 1) detects a/1. u/0 is not detected by these three patterns.

8. (5 points) Consider the combinational logic circuit below. How many possible single stuck-at faults does this circuit have? How many collapsed single stuck-at faults does this circuit have?



The number of possible faults is 2 x number_of_nets or 2 * 12 = 24. The number of collapsed faults = 2 x (number of POs + number of fanout stems) + total number of gate (including inverter) inputs – total number of inverters, in this case 2 * (1 + 3) + 8 – 0 = 16

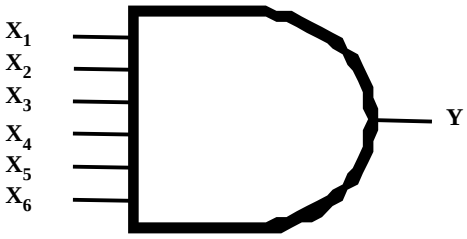
9. (5 points) Using the circuit shown, compute the detection ratio for d/1.

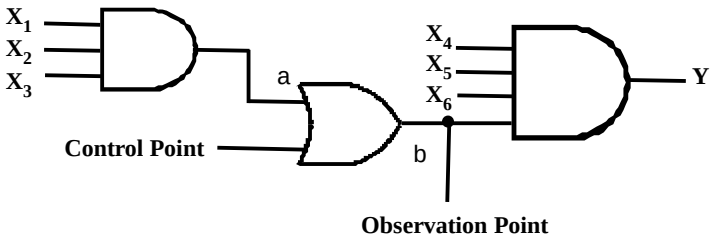


a	b	c	z ff	z d/1
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

The output is different for two input combinations, the detection ratio is 2/8 = 0.25.

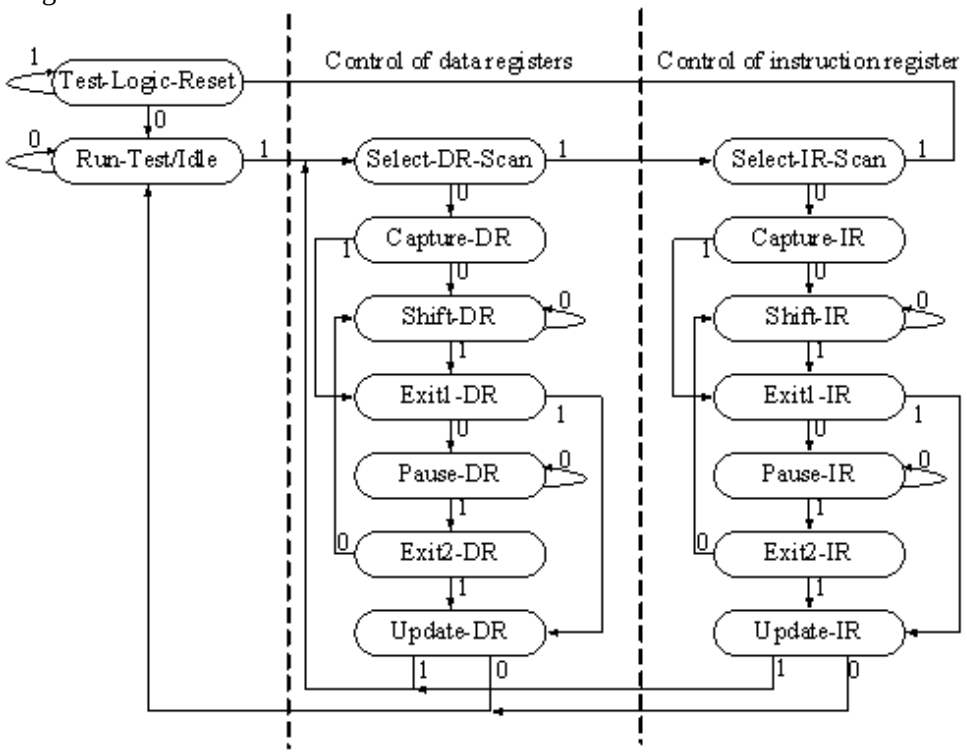
10. (5 points) For the circuit shown, calculate the detection probabilities, before and after test point insertion, for a s-a-1 fault present at Y.





Before test point insertion, P(Y = 0) = 1- P(Y = 1) = 1 – $(1/2)^6$ = 1 – 1/64 = 63/64. After test point insertion, P(Y = 0) = 1- P(Y = 1) is still true. In this case, P(Y = 1) = $(1/2)^3$P(b = 1). P(b = 1) = 1 – P(b = 0) = 1 – P(a = 0)P(CP = 0). P(a = 0) = 1- $(1/2)^3$ = 1 – 1/8 = 7/8. P(b = 0) = 7/8*1/2 = 7/16. P(b = 1) = 9/16. P(Y = 1) – 1/8*9/16 = 9/128.

11. (5 points) Assume that a 4-bit INTEST instruction is loaded into the instruction register of a boundary-scan architecture and the TAP is in the Select-DR-Scan state. Now you are going to apply 200 patterns to the internal logic and observe the test results. If the length of the boundary register is 20, then how many test cycles will be required to carry out the entire test procedure? Assume that the internal logic is a combinational circuit and that after the test procedure the circuit will return to the Test-Logic-Reset state.

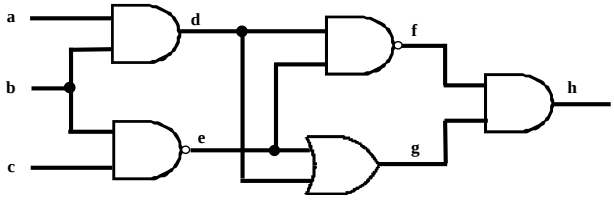


Assume the number of input wrapper cells equals that of output wrapper cells. The number of required test cycles to apply test patterns and propagate test responses is calculated as follows.

The number of required test cycles to apply a test pattern is 1 (to *Capture-DR*) + 1 (to *Shift-DR*)*10 + 1 (to *Exit1-DR*) + 1 (to *Update-DR*) +1 (to *Select-DR-Scan*) = 14
The number of required test cycles to observe test responses is 1 (to *Capture-DR*) + 1 (to *Shift-DR*)*10 + 1 (to *Exit1-DR*) + 1 (to *Update-DR*) + 1 (to *Select-DR-Scan*) = 14

Note that after the first test pattern is applied, applying test patterns and propagating test responses can be executed simultaneously. Therefore, the number of required test cycles to apply test patterns and propagate test responses will be 14 (applying the first test pattern) + 14*199 (applying test patterns and propagating test responses) + 14 (propagating the last test responses) + 1 (to *Select-IR-Scan*) + 1 (to *Test-Logic-Reset*) = 2816.

12. (5 points) Given the circuit shown. What are all the implications for e = 1?



The only implication for e = 1 is g = 1.

13. (10 points) Consider the dictionary of excited and detected stuck-at faults of a test set shown in the table below. Construct the smallest set of vectors that can detect as many transition faults as possible using only these five stuck-at vectors.

Vectors	Excited Faults	Detected Faults
V_1	a/0, b/1, c/0, d/0	c/0, e/1
V_2	c/0	e/1
V_3	d/0, e/0	a/0, b/1, c/1
V_4	a/0, b/0,	d/1, e/1
V_5	c/1, d/0	a/1, d/1

Pattern Pair	Delay Faults Detected	Pattern Pair	Delay Faults Detected
V_1-V_2	None	V_3-V_4	d slow-to-rise e slow-to-rise
V_2-V_3	c slow-to-rise	V_4-V_5	a slow-to-rise

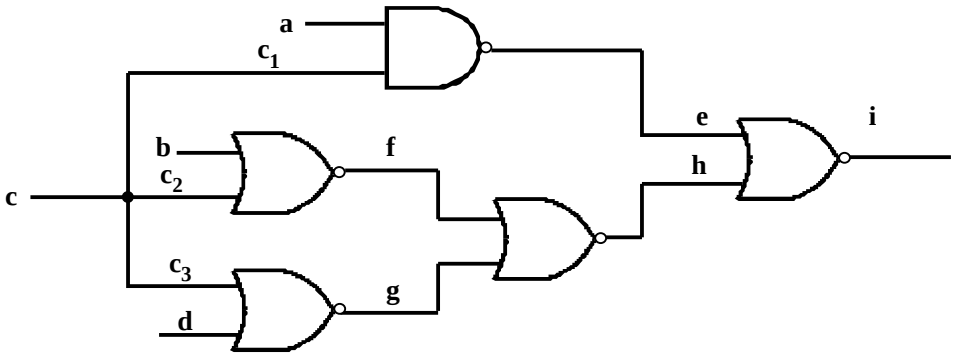
The faults that remain undetected after applying the five pattern sequence include:
a stf, b str, b stf, c stf, d stf, e stf , where stf is slow-to-fall and str is slow-to-rise

For these undetected faults, consider other vector pairs

Pattern Pair	Delay Faults Detected	Pattern Pair	Delay Faults Detected
V_1-V_3	None	V_5-V_1	c slow-to-fall
V_1-V_4	d slow-to-rise	V_5-V_2	None
V_1-V_5	a slow-to-rise, d slow-to-rise	V_5-V_3	None
		V_5-V_4	d slow-to-rise
V_2-V_1	None		
V_2-V_4	c slow-to-rise		
V_2-V_5	None		
V_3-V_1	e slow-to-rise		
V_3-V_2	e slow-to-rise		
V_3-V_5	d slow-to-rise		
V_4-V_1	None		
V_4-V_2	None		
V_4-V_3	b slow-to-rise		

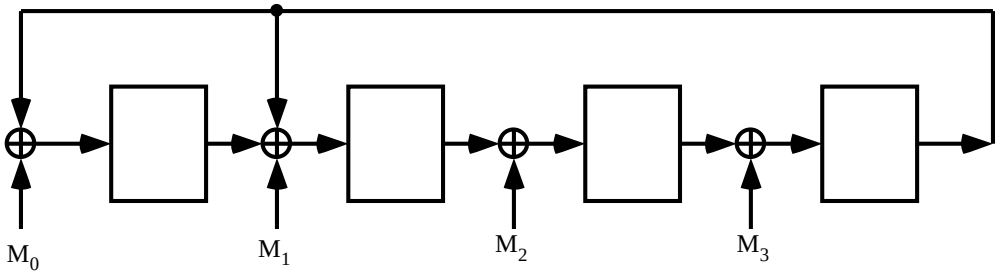
Two pattern pairs are needed to detect the additional detectable delay faults b str and c stf.
So, use {V_1, V_2, V_3, V_4, V_5, V_1, V_2, V_4}

14. (10 points) Using the circuit shown, use PODEM to compute a vector that can detect the fault h s-a-0.



Objective	Backtrace	Assignment	Implications	Decision Tree
(h, 1)	(f, 0), (g, 0), (b, 1), (d, 1)	b = 1	f = 0	b = 1
(h, 1)	(g, 0), (d, 1)	d = 1	g = 0, h = D'	b = 1, d = 1
(e, 0)	(a, 1), (c_1, 1), (c, 1)	a = 1		b = 1, d = 1, a = 1
(e, 0)	(c_1, 1), (c, 1)	c = 1	e = 0, i = D	b = 1, d = 1, a = 1, c = 1
Fault propagated to output, test pattern (a, b, c, d) = (1, 1, 1, 1)				

15. (10 points) Consider the four-stage MISR shown using $f(x) = 1 + x + x^4$. Let M_0 = {011011}, M_1 = {101101}, M_2 = {010101}, and M_3 = {011110}. Compute the fault-free signature. fault-free Then, compute the signature for the faulty sequences M_0' = {011100}, M_1' = {111101}, M_2' = {010111}, M_3' = {011111}. Explain why the faulty sequences are detected or not detected.



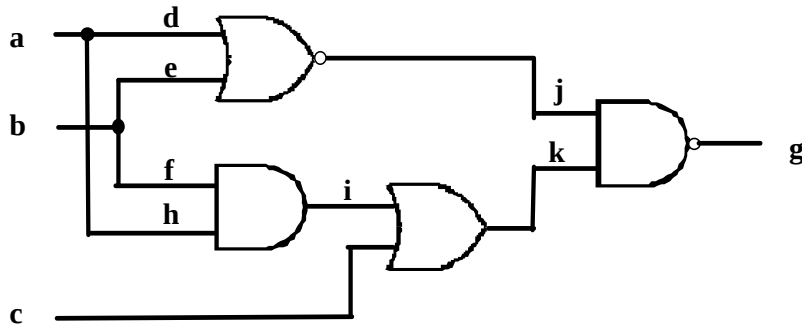
X0 = X3 ⊕ M0, X1 = X3 ⊕ X0 ⊕ M1, X2 = X1 ⊕ M2, X3 = X2 ⊕ M3

M0	M1	M2	M3	X0	X1	X2	X3
1	1	1	0	0	0	0	0
1	0	0	1	1	1	1	0
0	1	1	1	1	1	1	0
1	1	0	1	0	0	0	0
1	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
				1	0	0	0

M0	M1	M2	M3	X0	X1	X2	X3
0	1	1	1	0	0	0	0
0	0	1	1	0	1	1	1
1	1	1	1	1	1	0	0
1	1	0	1	1	0	0	1
1	1	1	1	0	1	0	1
0	1	0	0	0	0	0	1
				1	0	0	0

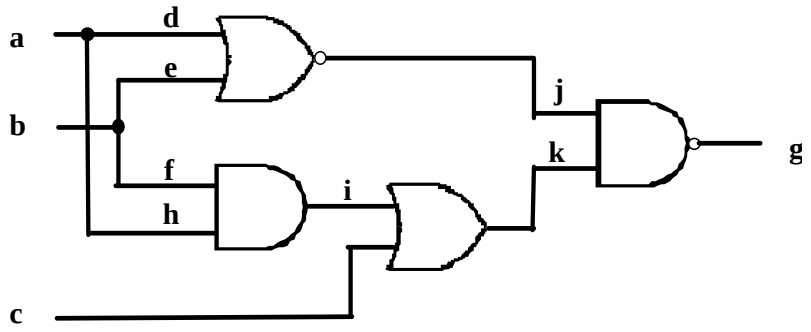
Because the two signatures are the same, the faulty sequences are not detected.

16. (10 points) For the circuit shown, calculate the probability-based controllabilities.



Line	0-C/1-C
a	_0.5/0.5_
b	_0.5/0.5_
c	_0.5/0.5_
d	_0.5/0.5_
e	_0.5/0.5_
f	_0.5/0.5_
h	_0.5/0.5_
i	_0.75/0.25_
j	_0.75/0.25_
k	_0.375/0.625_
g	_0.15625/0.84375_

17. (10 points) For the circuit shown and the SCOAP controllabilities given, calculate the SCOAP observabilities.



Line	CC0/CC1/CO
a	1/1/_7_
b	1/1/_5_
c	1/1/_7_
d	1/1/_5_
e	1/1/_5_
f	1/1/_7_
h	1/1/_7_
i	2/3/_5_
j	2/3/_3_
k	4/2/_4_
g	6/3/_0_