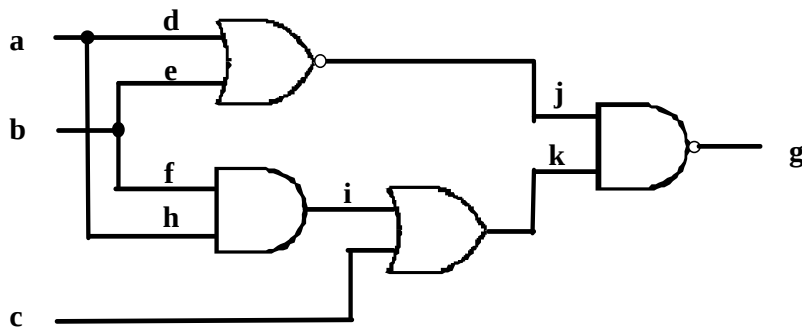
The University of Alabama in Huntsville
ECE Department
CPE 628 01
Test 2 Solution
Fall 2008

1. (10 points) For the circuit shown, compute all the vectors that can detect h s-a-1 using the Boolean difference.



$$\frac{df}{dh} = f(h=0) \oplus f(h=1)$$

$$f(h=0) = \overline{\overline{(a+b)} \bullet c} = \overline{\overline{(a+b)}} + \bar{c} = a + b + \bar{c}$$

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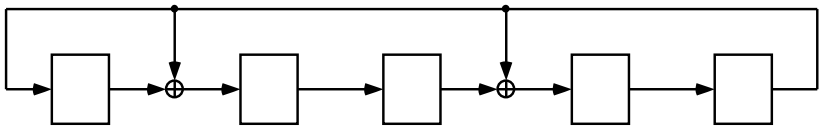
$f(h=0) \oplus f(h=1) = 0$, because f(h = 0) = f(h = 1).

To test for h s-a-1, use $\bar{h} \bullet \frac{df}{dh} = \bar{h} \bullet 0 = 0$. Therefore, h s-a-1 is redundant.

2. (5 points) List five different timing control schemes for BIST.

__one-hot single-capture, staggered single-capture, one-hot skewed-load, launch aligned skewed-load, capture aligned skewed-load, staggered skewed-load, one-hot double-capture, staggered double-capture, launch aligned double-capture, capture aligned double-capture, staggered double-capture _

3. (10 points) Consider the following LFSR. Generate the sequence starting with 00001. Is this a maximal LFSR? What is its length?

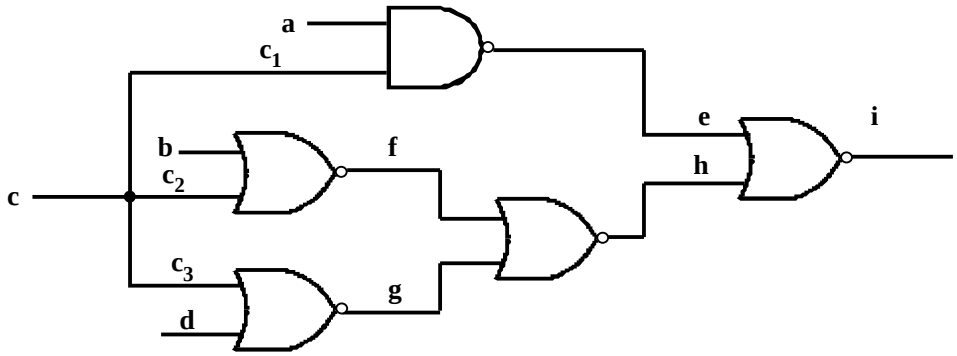


X1 = X5, X2 = X1 ⊕ X5, X3 = X2, X4 = X3 ⊕ X5, X5 = X4

X1	X2	X3	X4	X5	
0	0	0	0	1	
1	1	0	1	0	1
0	1	1	0	1	2
1	1	1	0	0	3
0	1	1	1	0	4
0	0	1	1	1	5
1	1	0	0	1	6
1	0	1	1	0	7
0	1	0	1	1	8
1	1	1	1	1	9
1	0	1	0	1	10
1	0	0	0	0	11
0	1	0	0	0	12
0	0	1	0	0	13
0	0	0	1	0	14
0	0	0	0	1	15

The length is 15 which is not maximal.

4. (15 points) For the circuit given,
   a. Compute the static logic implications of c = 0.
   b. Compute the static logic implications of c = 1.
   c. Compute the set of faults that are untestable when c = 0.
   d. Compute the set of faults that are untestable when c = 1.
   e. Compute the set of untestable faults based on the stem analysis of c.



a. c = 0 implies $c_1 = 0$, $c_2 = 0$, $c_3 = 0$, e = 1, i = 0

b. c = 1 implies c_1 = 1, c_2 = 1, c_3 = 1, f = 0, g = 0, h = 1, i = 0

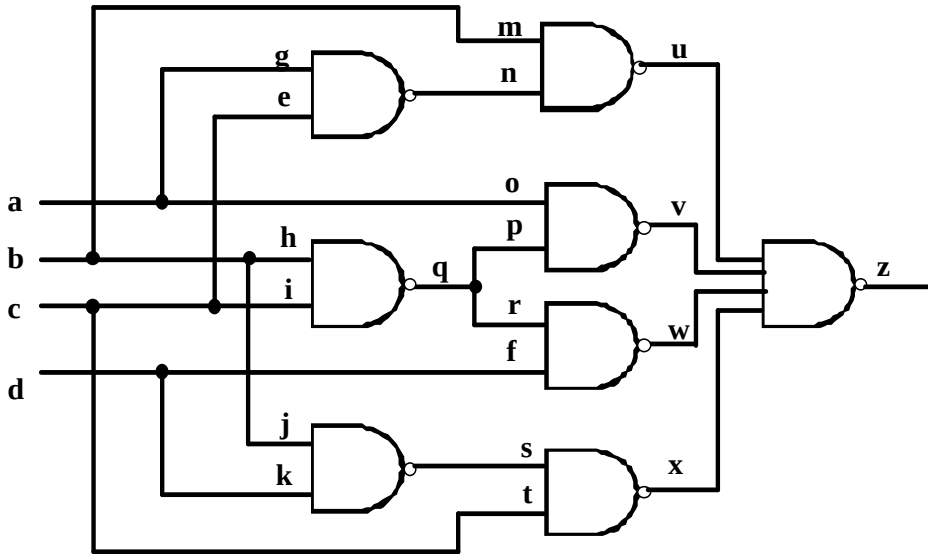
c. Unexcitable: c/0, c_1/0, c_2/0, c_3/0, e/1, i/0
Unobservable: a/0, a/1, b/0, b/1, c_2/0, c_2/1, c_3/0, c_3/1, d/0, d/1, f/0, f/1, g/0, g/1, h/0, h/1
Untestable: a/0, a/1, b/0, b/1, c/0, c_1/0, c_2/0, c_2/1, c_3/0, c_3/1, d/0, d/1, e/1, f/0, f/1, g/0, g/1, h/0, h/1, i/0

d. Unexcitable: c/1, c_1/1, c_2/1, c_3/1, f/0, g/0, h/1, i/0
Unobservable: a/0, a/1, b/0, b/1, c_1/0, c_1/1, d/0, d/1, e/0, e/1
Untestable: a/0, a/1, b/0, b/1, c/1, c_1/0, c_1/1, c_2/1, c_3/1, d/0, d/1 e/0, e/1, f/0, g/0, h/1, i/0

e. Untestable = Untestable (c = 0) ∩ Untestable (c = 1) = a/0, a/1, b/0, b/1, c_1/0, c_2/1, c_3/1, d/0, d/1, e/1, f/0, g/0, h/1, i/0

5. (1 point) _Compaction_ is a method for dramatically reducing the number of bits in the original circuit response during testing in which some information is lost.

6. (15 points) Using the circuit shown, use PODEM to compute a vector that can detect the fault q s-a-1.

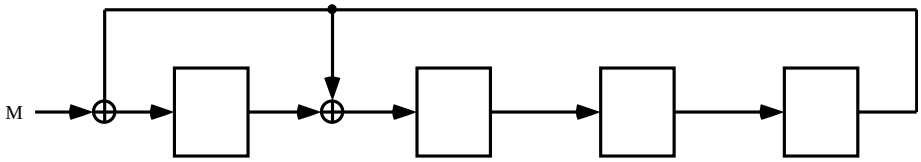


Objective	Backtrace	Assignment	Implications	Decision Tree
(q, 0)	(h, 1), (i, 1), (b, 1), (c, 1)	b = 1	m = 1, h = 1, j = 1	b = 1
(q, 0)	(i, 1), (c, 1)	c = 1	e = 1, i = 1, q = D', p = D', r = D', t = 1	b = 1, c = 1
(o,1), pick from D-frontier	(a, 1)	a = 1	g = 1, o = 1, n = 0, u = 1, v = D	b = 1, c = 1, a = 1
(w, 1)	(d, 0)	d = 0	f = 0, k = 0, s = 1, x = 0, z = 1, w = 1, no possible path	b = 1, c = 1, a = 1, d = 0
(f, 1), pick other option from D-frontier	(d, 1)	d = 1	F = 1, w = D, k = 1, s = 0, x = 1, z = D'	b = 1, c = 1, a = 1, d = 1
Fault Detected, test vector is (a, b, c, d) = 1111				

7. (1 point) The Logic BIST system most used in industry is named _STUMPS_.

8. (1 point) An _intra-domain_ fault originates at one clock domain and terminates at the same clock domain.

9. (15 points) Compute the signature of the SISR using $f(x) = 1 + x + x^4$ given for the fault-free sequence M = {110110010101011}. Then, compute the signature for the faulty sequence M' = {111100001100101}. Explain why M' is detected or not detected.



R0 = M ⊕ R3, R1 = R0 ⊕ R3, R2 = R1, R3 = R2

M	R0	R1	R2	R3
	0	0	0	0
1	1	0	0	0
1	1	1	0	0
0	0	1	1	0
1	1	0	1	1
0	1	0	0	1
1	0	0	0	0
0	0	0	0	0
1	1	0	0	0
0	0	1	0	0
0	0	0	1	0
1	1	0	0	1
1	0	0	0	0
0	0	0	0	0
1	1	0	0	0
1	1	1	0	0

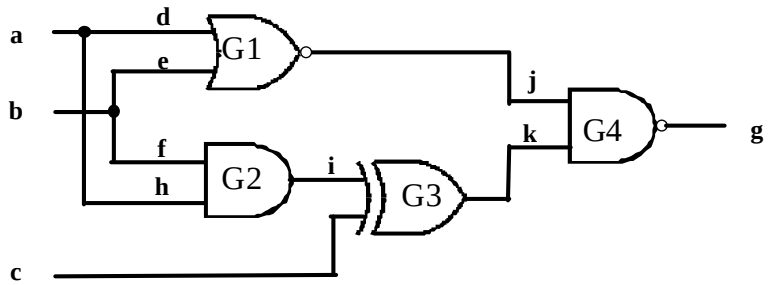
M	R0	R1	R2	R3
	0	0	0	0
1	1	0	0	0
0	0	1	0	0
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1
1	0	0	1	1
0	1	1	0	1
0	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0

Since R' is not equal to R, the faulty sequence is detected.

10. (1 point) For aligned skewed-load testing a clock _suppression_ circuit is used to enable or disable selected shift or capture pulses.

11. (1 point) One type of delay fault test is known as a _robust_ delay test.

12. (10 points) For the circuit shown, use the D algorithm to compute a test vector for the fault i s-a-1.



a	b	c	d	e	f	h	i	j	k	g	D-frontier	J-frontier
X	X	X	X	X	X	X	X	X	X	X		
					0	X	D’					
X	X	X	X	X	0	X	D’	X	X	X	G3	f
		0					D’		D’			
X	X	0	X	X	0	X	D’	X	D’	X	G4	f
								1	D’	D		
X	X	0	X	X	0	X	D’	1	D’	D		f, j
	0			0	0							
X	0	0	X	0	0	X	D’	1	D’	D		j
			0	0				1				
X	0	0	0	0	0	X	D’	1	D’	D		d
0			0			0						
0	0	0	0	0	0	0	D’	1	D’	D		

13. (15 points) For the circuit shown, insert two test points so the minimum detection probability for any fault in the circuit is greater than or equal to 1/16 and draw the resulting circuit. Assume control points are randomly activated.