The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Fall 2013
Final Exam Solution

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

1. (1 point) A _**counter**_ is essentially a register that goes through a predetermined sequence of binary states.
2. (1 point) A _**characteristic equation**_ specifies the next state as a function of the present state and inputs.
3. (1 point) Moore and Mealy models of a sequential circuit are commonly referred to as a _**finite state machines**_,
4. (1 point) List one keyword found in a Verilog model _**module, wire, input, output, etc.**_.
5. (1 point) _**Complements**_ are used in digital computers to simplify the subtraction operation and for logical manipulation.
6. (5 points Convert (6401325_7) to decimal:

   $6401325_7 = 6 \times 7^6 + 4 \times 7^5 + 0 \times 7^4 + 1 \times 7^3 + 3 \times 7^2 + 2 \times 7^1 + 5 \times 7^0 = 773{,}631$

7. (10 points) Convert decimal +273 and +451 to binary, using the signed-2's-complement representation and enough digits to accommodate the numbers. Then perform the binary equivalent of (+273) + (-451). Convert the answer back to decimal and verify that it is correct.

   +273 = 1 × -512 + 1 × 256 0 × 128 + 0 × 64 + 0 × 32 + 1 × 16 + 0 × 8 + 0 × 4 + 0 × 2 + 1 × 1
   = 00 0010 0101
   +451 = 1 × -512 + 0 × 256 0 × 128 + 1 × 64 + 0 × 32 + 1 × 16 + 0 × 8 + 0 × 4 + 1 × 2 + 0 × 1
   = 0101 0010

   -451 = 1 × -512 + 0 × 256 + 0 × 128 + 0 × 64 + 1 × 32 + 1 × 16 + 1 × 8 + 1 × 4 + 0 × 2 + 1 × 1 =
   10 0011 1101

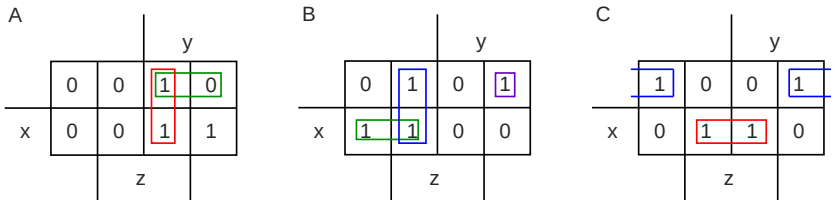
   +273 01 0001 0001
   -451 10 0011 1101
   11 0100 1110
   11 0001 1000 = 1 × -512 + 1 × 256 + 0 × 128 + 1 × 64 + 0 × 32 + 0 × 16 + 1 × 8 + 1 × 4 + 1 × 2 +
   0 × 1 = -128 + 8 + = -178 ✓

8. (10 points) How many 2-to-4 line decoders with enable does it take to construct an 8-to-256 line decoder?

At the output level, 256/4 = 64 decoders are required.
Moving towards the input, the next level requires 64/4 = 16 decoders
Still moving towards the input, the next level requires 16/4 = 4 decoders
Once more, 4/1 = 1 decoder
Total = 64 + 16 +4 +1 = 85 decoders

9. (10 points) Design a circuit with inputs x, y, and z and outputs A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

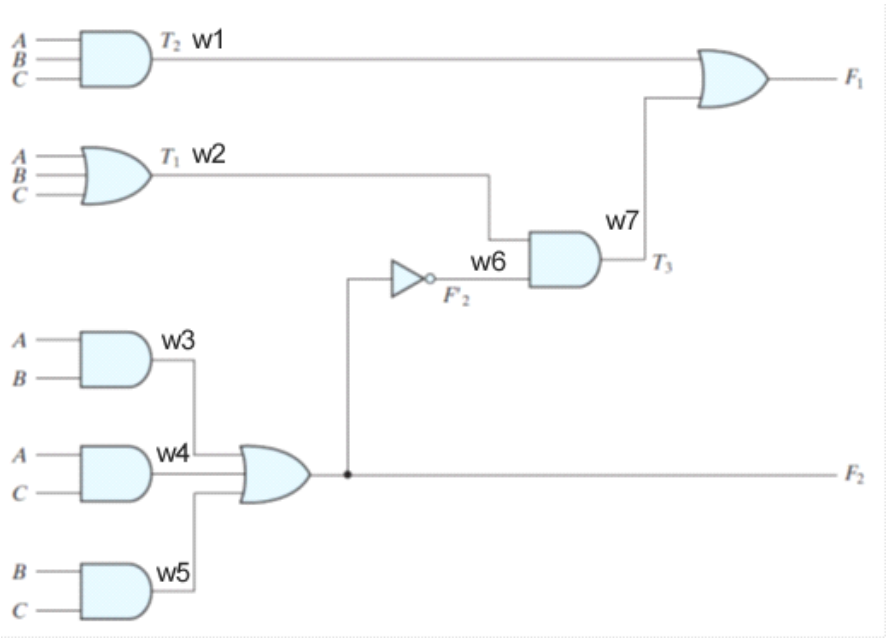


A = **yz** + **x'y**

B = **xy'** + **y'z** + **x'yz'**

C = **xz** + **x'z'**

10. (10 points) Write a Verilog gate-level description of the circuit shown.




```
module Circuit (F1, F2, A, B, c);
  input   A, B, C;
  output  F1, F2;
  wire    w1, w2, w3, w4, w5, w6, w7;
  and     (w1, A, B, C);
  or      (w2, A, B, C);
  and     (w3, A, B);
  and     (w4, A, C);
  and     (w5, B, C);
  or      (F2, w3, w4, w5);
  not     (w6, F2);
  and     (w7, w2, w6);
  or      (F1, w1, w7);
endmodule
```

11. (10 points) Reduce the number of states in the following state table, and tabulate the reduced state table:

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	**d**	**c**	**0**	**0**
c	f	e	0	0
d	**g**	**a**	**1**	**0**
e	**d**	**c**	**0**	**0**
f	f	b	1	1
g	g	h	0	1
h	**g**	**a**	**1**	**0**

b = e and d = h

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	**f**	**b**	**0**	**0**
b	d	c	0	0
c	**f**	**b**	**0**	**0**
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

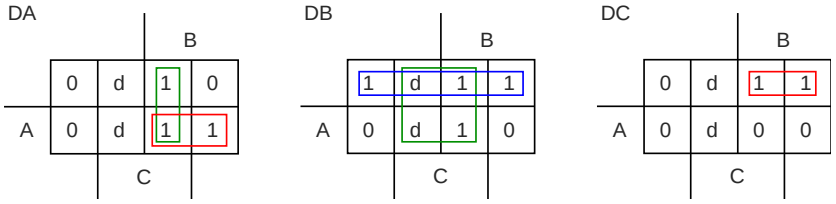
a = c

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	d	a	0	0
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

12. (15 points) Design a 3-bit counter which counts in the sequence 000, 010, 011, 111, 110, 100, 000 using clocked D flip-flops. You do not have to draw the circuit diagram. Is the counter self-correcting if it comes up in an unused state?

Q	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	DA	DB	DC
000	**010**	**0**	**1**	**0**
010	**011**	**0**	**1**	**1**
011	**111**	**1**	**1**	**1**
111	**110**	**1**	**1**	**0**
110	**100**	**1**	**0**	**0**
100	**000**	**0**	**0**	**0**



D_A = **AB + Bx** D_B = **A' + C** D_C = **A'B**

13. (25 points) A Moore sequential circuit has one input and one output. When the input sequence 011 occurs, the output becomes 1 and remains 1 until the sequence 011 occurs again in which case the output returns to 0. The output then remains 0 until 011 occurs a third time, etc. For example, the input sequence

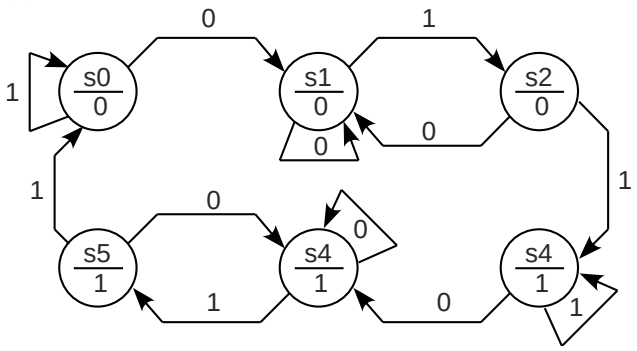
X = 01011010110100111

has the output

Z = 00001111100000011

(a) (8 points) Draw the state diagram for this circuit.
(b) (4 points) Draw the state table.
(c) (5 points) Derive the excitation for implementing this circuit with T flip-flops.
(d) (8 points) Derive the equations for the inputs of the T flip-flops.

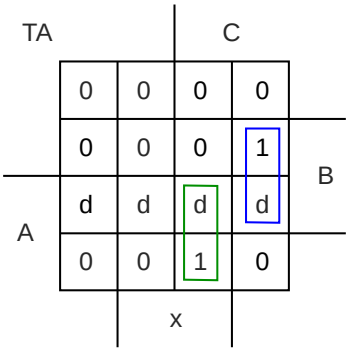
(a)

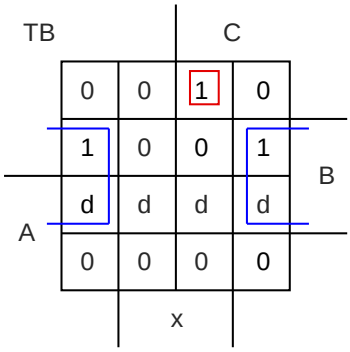


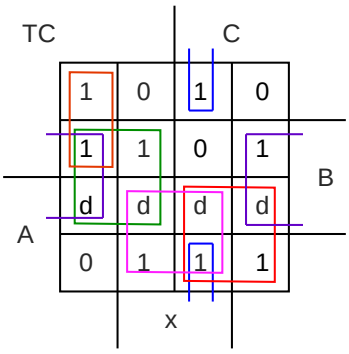
(b), (c)

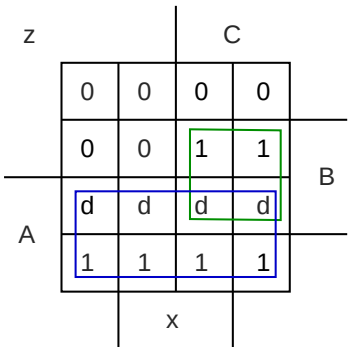
PS			x		NS				TA	TB	TC		z
0	0	0	0		0	0	1		0	0	1		0
0	0	0	1		0	0	0		0	0	0		0
0	0	1	0		0	0	1		0	0	0		0
0	0	1	1		0	1	0		0	1	1		0
0	1	0	0		0	0	1		0	1	1		0
0	1	0	1		0	1	1		0	0	1		0
0	1	1	0		1	0	0		1	1	1		1
0	1	1	1		0	1	1		0	0	0		1
1	0	0	0		1	0	0		0	0	0		1
1	0	0	1		1	0	1		0	0	1		1
1	0	1	0		1	0	0		0	0	1		1
1	0	1	1		0	0	0		1	0	1		1

(d)









TA = **ACx** + **BCx'** TB = **Bx'** + **A'B'Cx** TC = **Ax** + **AC** + **BC'** + **Bx'** + **B'Cx** + **A'C'x'**

Z = **A** + **BC**