

The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Fall 2013
Test 2
October 29, 2013

Name: _____

1. (1 point) A _____ is a diagram made up of squares representing one minterm of the function that is to be minimized.
2. (1 point) When two numbers with n digits each are added and the sum is a number occupying n + 1 digits, we say that an _____ occurred.
3. (1 point) _____.(True/False) When minimizing a function, all don't care terms must be included.
4. (1 point) A _____.is a product term obtained by combining the maximum possible number of adjacent squares in the map.
5. (1 point) The implementation of Boolean functions with NAND gates requires that the functions be in _____ form.
6. (10 points) Simplify the following function and implement it with two-level NOR gates:
$$F(x, y, z) = x'z' + y'z' + yz' + xy$$

7. (20 points) Design a circuit that has four inputs $w, x, y,$ and z and four outputs $A, B, C,$ and D . $wxyz$ represents a binary-coded decimal digit. AB represents the quotient and CD the remainder when $wxyz$ is divided by 3 (AB and CD represent 2-bit unsigned binary numbers. Output $ABCD = 1111$ if an invalid value appears on the inputs. You do not have to draw a circuit diagram.

8. (15 points) Find all the prime implicants for the following Boolean function, and determine which are essential:

$$F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$$

9. (10 points) Simplify the following Boolean function, using four-variable maps:

$$F(w, x, y, z) = \Sigma(4, 12, 7, 2, 10)$$

$$d(w, x, y, z) = \Sigma(0, 6, 8)$$

10. (15 points) Draw the logic diagram of the digital circuit specified by the following Verilog description:

```
module Circuit_B (F1, F2, A0, A1, B0, B1);
    input    A0, A1, B0, B1;
    output   F1, F2;
    wire     w1, w2, w3, w4, w5, w6, w7;
    or       (F1, w1, w2, w3);
    and (F2, w4, w5);
    and (w1, w6, B1);
    or      (w2, w6, w7, B0);
    and (w3, w7, B0, B1);
    not (w6, A1);
    not (w7, A0);
    xor (w4, A1, B1);
    xnor (w5, A0, B0);
endmodule
```

11. (10 points) Write a Verilog gate-level description of the circuit for F in problem 12, including delays.

12. (15 points) If the delays in the circuit below are as given in the table, find the propagation delays from the inputs to F and $F_{\text{simplified}}$.

Logic Element	Propagation Delay
Inverter	30 ps
AND/NAND	50 ps
OR/NOR	60 ps
XOR	80 ps
Full Adder	150 ps

