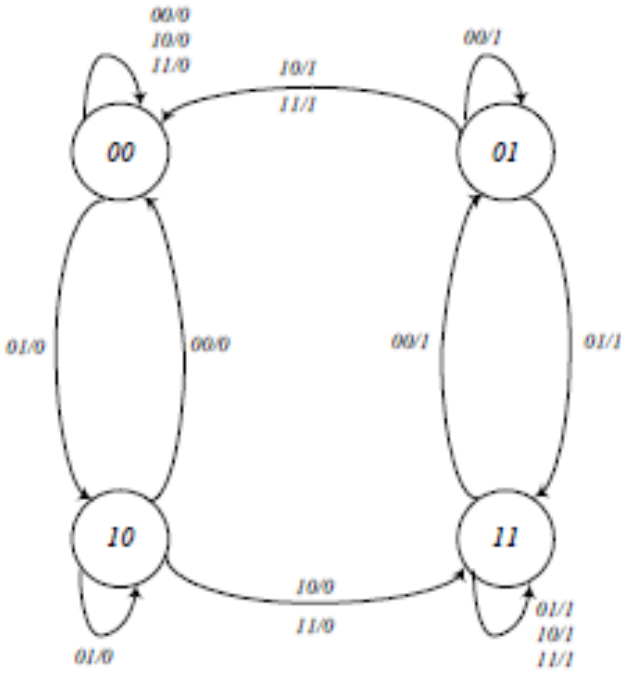
The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Test 3 Solution
Fall 2013

1. (1 point) Storage elements that operate with signal levels (rather than signal transitions) are referred to as _**latches**_.
2. (1 point) A _**characteristic table**_ defines the logical properties of a flip-flop by describing its operation in tabular form.
3. (1 point) Some flip-flops have _**asynchronous**_ inputs that are used to force the flip-flop to a particular state independent of the clock.
4. (1 point) The time sequence of inputs, outputs, and flip-flop states can be enumerated in a _**state table**_.
5. (1 point) In Verilog, behavior declared by the keyword **initial** is called _**single pass**_ behavior.
6. (15 points) Starting from state 00 in the state diagram shown, determine the state transitions and output sequence that will be generated when an input sequence of 00, 11, 10, 01, 11, 10, 01, 00, 10, 10, 00, 01, 01, 11, 11, 00, 00



Current State	Input	Next State	Output
00	00	00	0
00	11	00	0
00	10	00	0
00	01	10	0
10	11	11	0
11	10	11	1
11	01	11	1
11	00	01	1
01	10	00	1
00	10	00	0
00	00	00	0
00	01	10	0
10	01	10	0
10	11	11	0
11	11	11	1
11	00	01	1
01	00	01	1

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

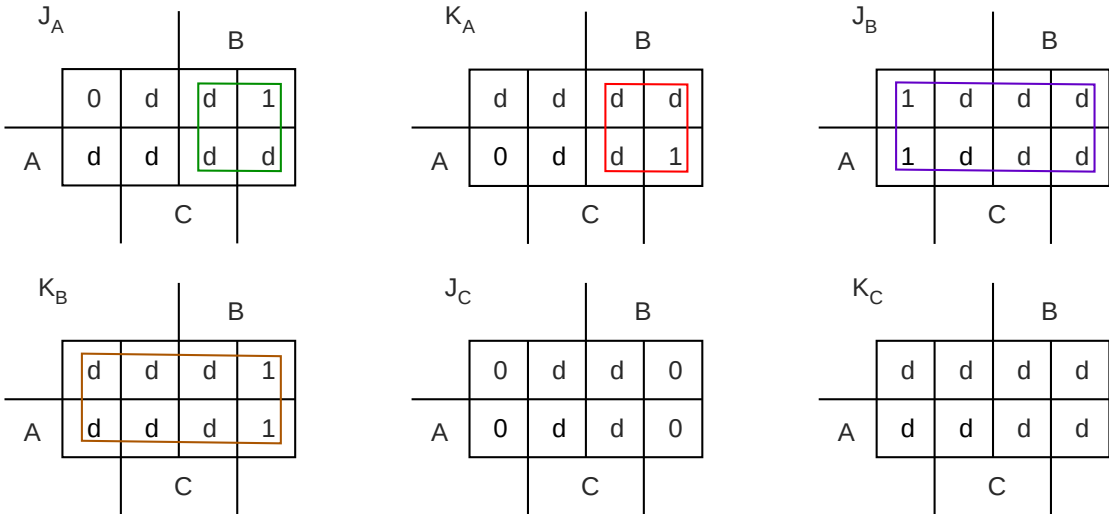
D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

7. (20 points) Design a 3-bit counter which counts in the sequence 000, 010, 100, 110, 000 using clocked JK flip-flops. You do not have to draw the circuit diagram. What will happen if the counter is started in state 101?

Q	Q(t+1)	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

Present State	Next State	JA	KA	JB	KB	JC	KC
000	**010**	**0**	**d**	**1**	**d**	**0**	**d**
010	**100**	**1**	**d**	**d**	**1**	**0**	**d**
100	**110**	**d**	**0**	**1**	**d**	**0**	**d**
110	**000**	**d**	**1**	**d**	**1**	**0**	**d**



$J_A = B$ **$K_A = B$** **$J_B = 1$** **$K_B = 1$** **$J_C = 0$** **$K_C = 0$**

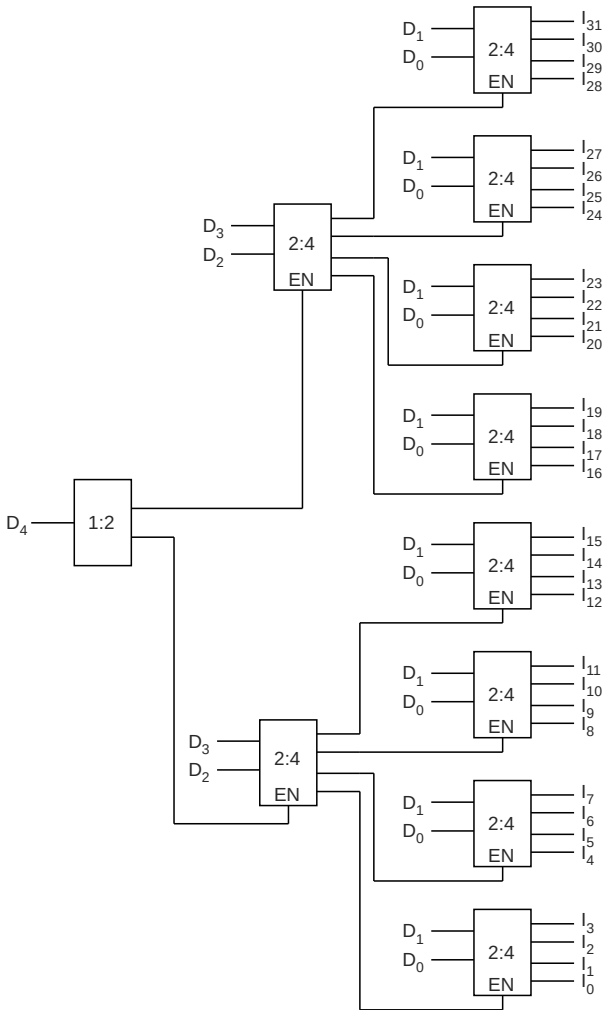
From state 101, $J_A = 0$, $K_A = 0$, $J_B = 1$, $K_B = 1$, $J_C = 0$, $K_C = 0$, A stays the same at 1, B toggles to 1 and C stays the same at 1, so the next state from 101 is 111

8. (10 points) Reduce the number of states in the following state table, and tabulate the reduced state table:

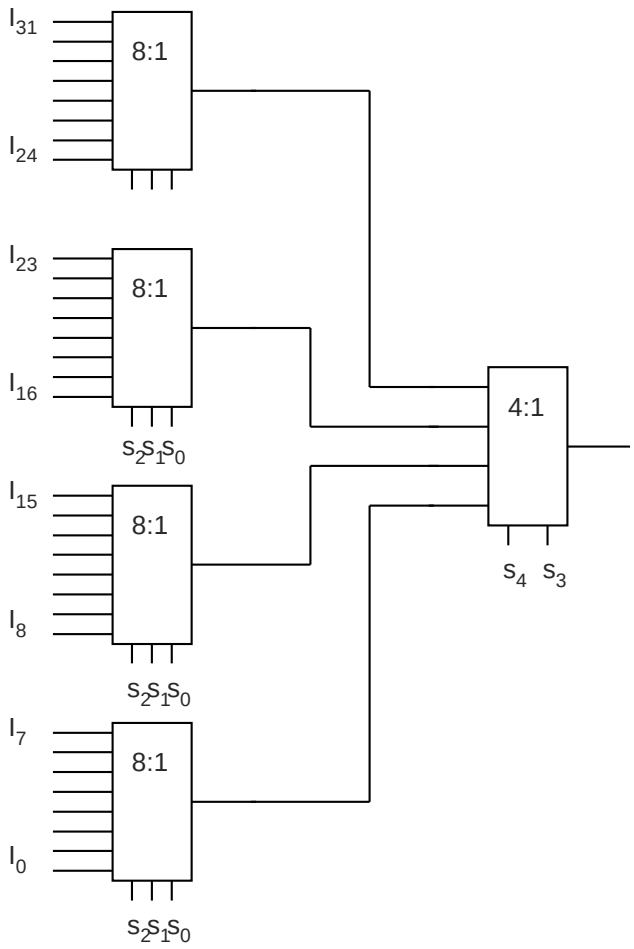
Present State	Next State		Present Output (Z)
	x = 0	x = 1	
a	e	e	1
b	c	e	1
c	i	h	0
d	h	a	1
e	i	f	0
f	e	g	0
g	h	b	1
h	c	d	0
i	f	b	1

None of the states have the same next states and outputs, this table is already in its reduced form.

9. (15 points) Construct a 5-to-32 line decoder using as many 2-to-4 line decoders with enable and any additional logic that you might need. Use block diagrams for the components.

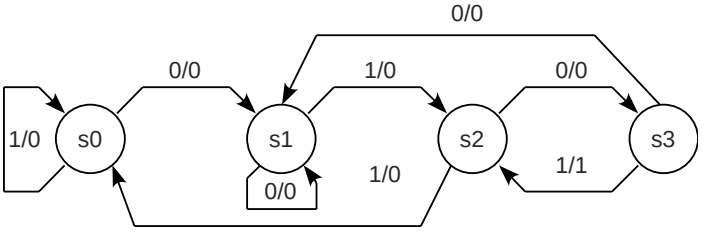


10. (10 points) Construct a 32 × 1 multiplexer using as many 8 × 1 multiplexers and any additional logic that you might need. Use block diagrams for the components.



11. (25 points) Design a Mealy sequential circuit that has an output of 1 whenever its input string has the sequence 0101 and otherwise has an output of 0. These sequences can overlap. Use T flip-flops. You do not have to draw the circuit diagram.

Input: 00101011101000111110101010111000011001
Output: 00001010000000000000001010100000000000



Present State	x	Next State	TA	TB	z
00	**0**	**01**	**0**	**1**	**0**
00	**1**	**00**	**0**	**0**	**0**
01	**0**	**01**	**0**	**0**	**0**
01	**1**	**10**	**1**	**1**	**0**
10	**0**	**11**	**0**	**1**	**0**
10	**1**	**00**	**1**	**0**	**0**
11	**0**	**01**	**1**	**0**	**0**
11	**1**	**10**	**0**	**1**	**1**

TA

A \ B	0	1
0	0	1
1	0	1

x

TA = AB'x + A'Bx + ABx'

TB

A \ B	0	1
0	1	1
1	0	0

x

TB = Bx + B'x'

z

A \ B	0	1
0	0	0
1	0	1

x

z = ABx