The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Fall 2016
Final Exam Solution

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

1. (1 point)._**VHDL/Verilog**_ is an example of a hardware description language.
2. (1 point) _**False**_ (True/False) Modern processors are designed using K-maps.
3. (1 point) _**False**_ (True/False) The outputs in a Moore machine depend on the current state and the inputs.
4. (1 point) A register that goes through a prescribed sequence of states upon the application of input pulses is called a _**counter**_
5. (1 point) A _**Karnaugh map**_ is a pictorial form of a truth table.

6. (5 points Convert (578.134_9) to decimal.

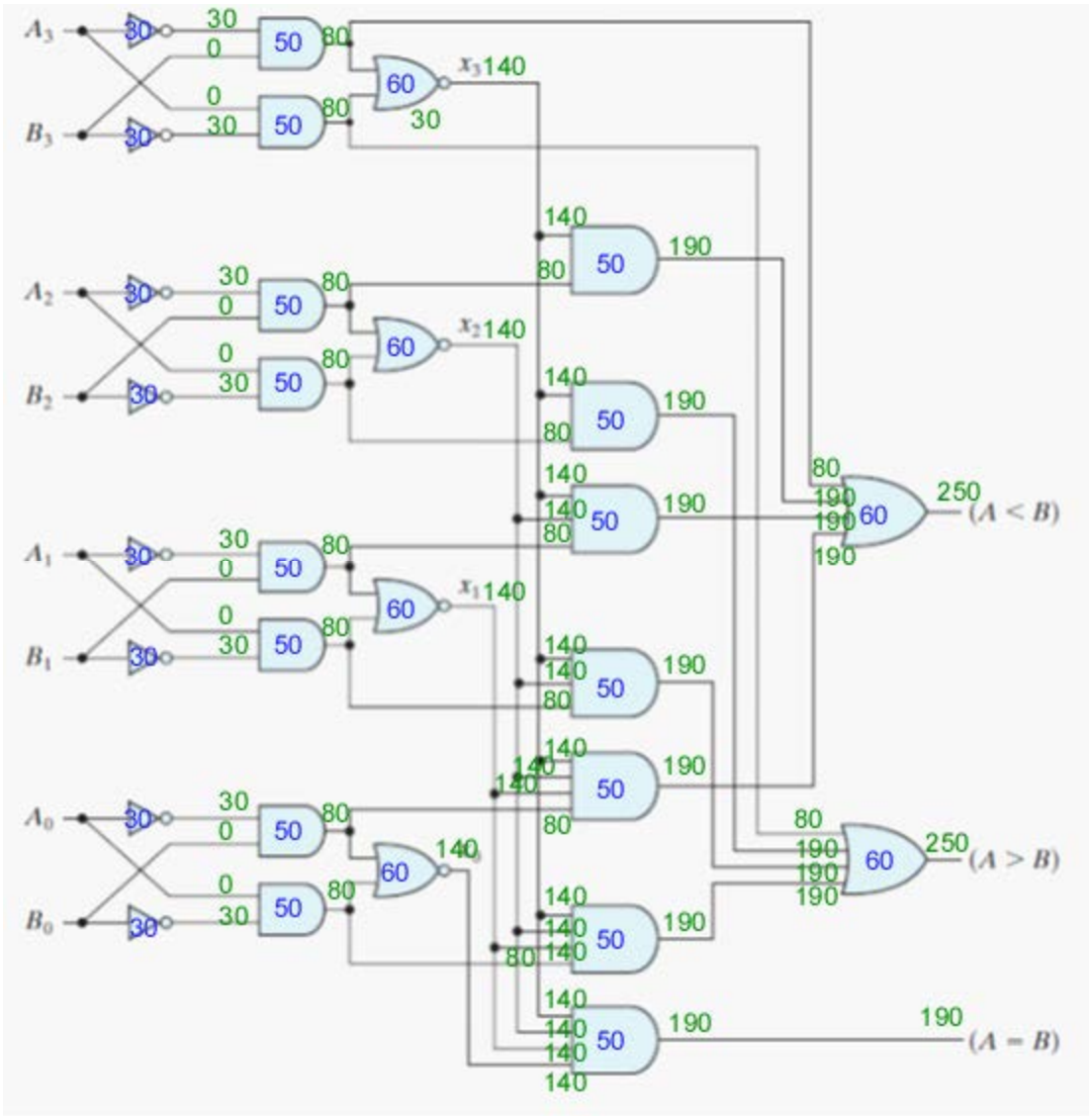
   $5 \times 9^2 + 7 \times 9^1 + 8 \times 9^0 + 1 \times 9^{-1} + 3 \times 9^{-2} + 4 \times 9^{-3} =$
   $5 \times 81 + 7 \times 9 + 8 \times 1 + 1 \times 0.1111 + 3 \times 0.01235 + 4 \times 0.001372 =$
   $405 + 63 + 8 + 0.1111 + 0.037 + 0.00549 = 476.154$

7. (10 points) How many 2 x 1 multiplexers does it take to make a 128 x 1 multiplexer?

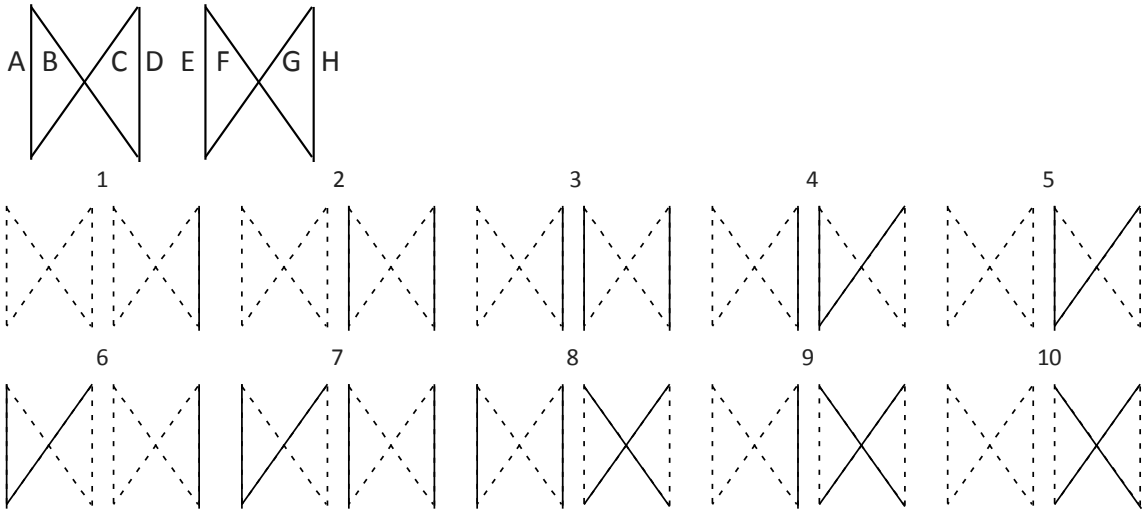
   At the first level, 128/2 (64) multiplexers are needed, leaving 64 inputs for the next level
   At the second level, 64/2 (32) multiplexers are needed, leaving 32 inputs for the next level
   At the third level, 32/2 (16) multiplexers are needed, leaving 16 inputs for the next level
   At the fourth level, 16/2 (8) multiplexers are needed, leaving 8 inputs for the next level
   At the fifth level, 8/2 (4) multiplexers are needed, leaving 4 inputs for the next level
   At the sixth level, 4/2 (2) multiplexers are needed, leaving 2 inputs for the next level
   At the seventh level, 2/2 (1) multiplexers are needed, providing the final output
   The total number of multiplexers is 64 + 32 + 16 + 8 + 4 + 2 + 1 = 127

8. (10 points) If the delays in the circuit below are as given in the table, find the propagation delays from the inputs to A < B, A > B, and A = B.

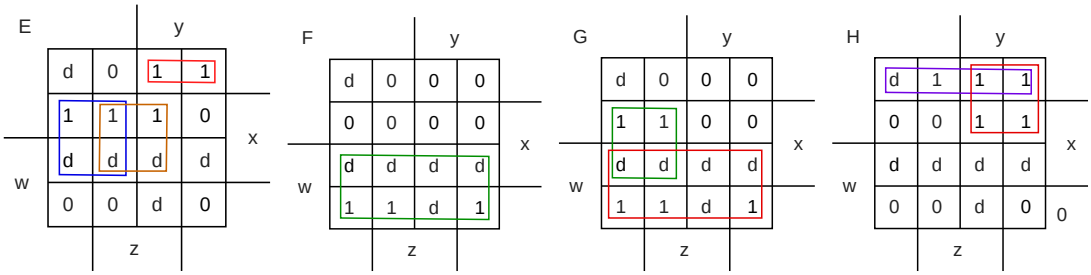
Logic Element	Propagation Delay
Inverter	30 ps
AND/NAND	50 ps
OR/NOR	60 ps
XOR	80 ps
Full Adder	150 ps



9. (15 points) Consider a system which has as its inputs a number from 1 to 10 and provides as its outputs (eight of them) the signals to drive the following display. The inputs are labeled w, x, y, and z and are normal binary. The input combinations 0000, 1011, 1100, 1101, 1110, and 1111 will never occur; they are to be treated as don't cares. The display allows for the representation of Roman numerals (except that IIX is used to represent 8, whereas it is normally written as VIII). There are a total of eight segments in the display, labeled A through H, as shown. To light a segment, a 1 is placed on the appropriate display input (A, B, C, D, E, F, G, H). The following illustration shows all digits as they should be coded for each of these, with a lit segment represented by a bold line and an unlit segment represented by a dashed line. Derive the equations for the circuitry for E, F, G, and H.



w	x	y	z	A	B	C	D	E	F	G	H
0	0	0	0	d	d	d	d	d	d	d	d
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	1	0	0	1
0	0	1	1	0	0	0	1	1	0	0	1
0	1	0	0	0	0	0	1	1	0	1	0
0	1	0	1	0	0	0	0	1	0	1	0
0	1	1	0	1	0	1	0	0	0	0	1
0	1	1	1	1	0	1	0	1	0	0	1
1	0	0	0	1	0	0	1	0	1	1	0
1	0	0	1	1	0	0	1	0	1	1	0
1	0	1	0	0	0	0	0	0	1	1	0
1	0	1	1	d	d	d	d	d	d	d	d
1	1	0	0	d	d	d	d	d	d	d	d
1	1	0	1	d	d	d	d	d	d	d	d
1	1	1	0	d	d	d	d	d	d	d	d
1	1	1	1	d	d	d	d	d	d	d	d



E = **xy'** + **xz** + **w'x'y** F = **w** G = **xy'** + **w** H = **w'y** + **w'x'**

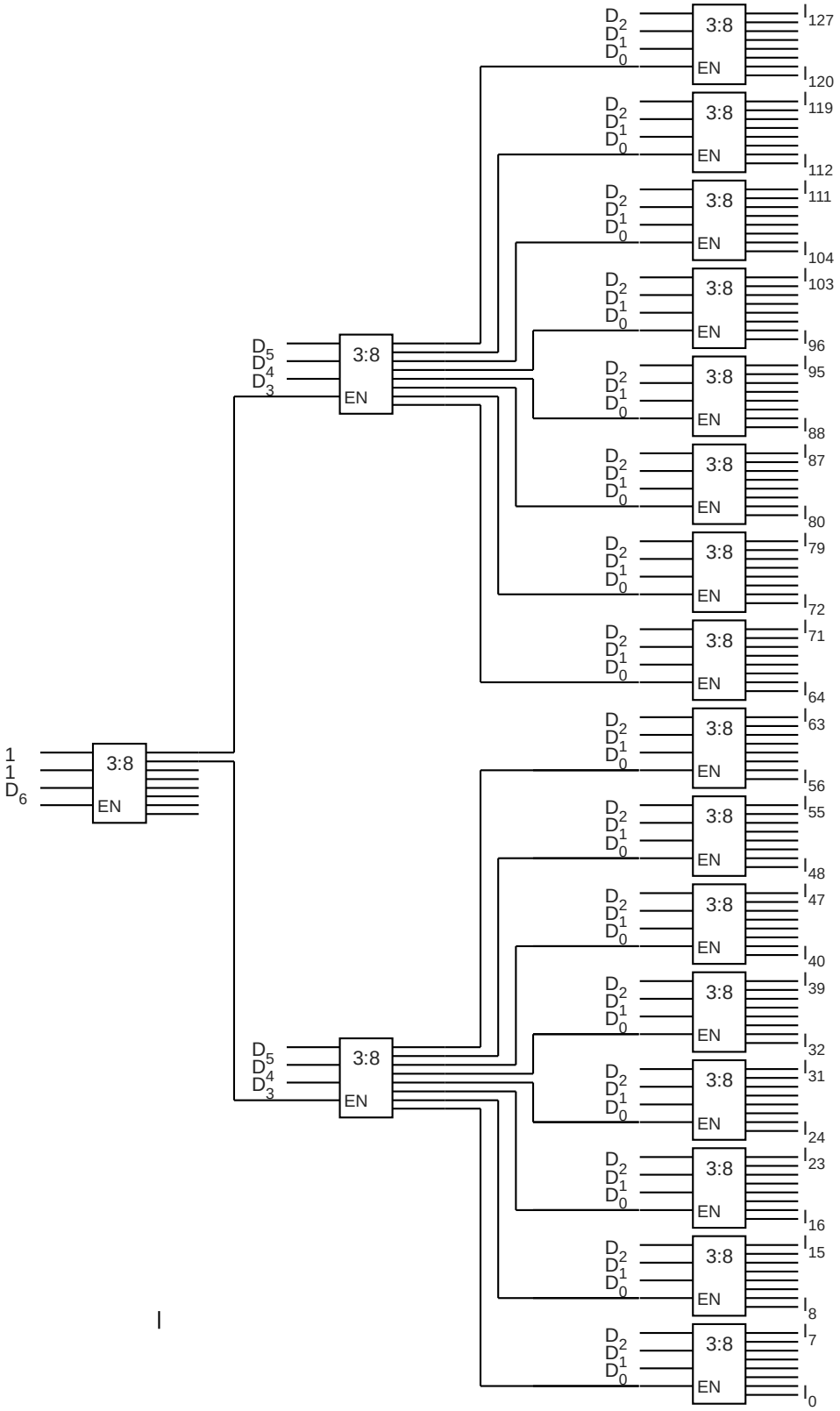
10. (10 points) Convert decimal -53 and +109 to binary, using 8-bit signed-2's-complement representation. Then perform the binary equivalent of (-53) + (109). Convert the answer back to decimal and verify that it is correct or explain why it is not.

-53 = 1 × -128 + 1 × 64 + 0 × 32 + 0 × 16 + 1 × 8 + 0 × 4 + 1 × 2 + 1 × 1 = 1100 1011
+109 = 0 × -128 + 1 × 64 + 1 × 32 + 0 × 16 + 1 × 8 + 1 × 4 + 0 × 2 + 1 × 1 = 0110 1101

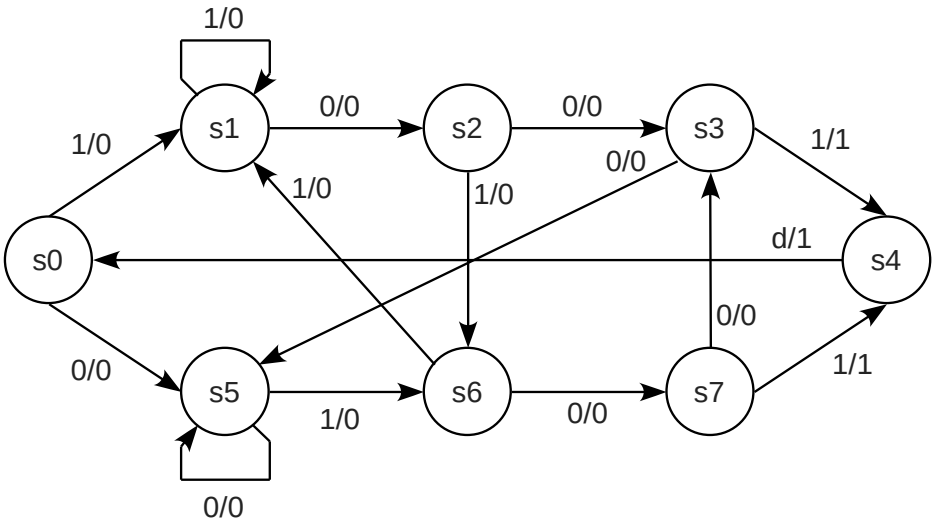
-53 1100 1011
+109 0110 1101
0011 1000
0011 1000 =0 × -128 + 0 × 64 + 1 × 32 + 1 × 16 + 1 × 8 + 0 × 4 + 0 × 2 + 0 × 1 =
32 + 16 + 8 = 56 ✓

The result matches because the result falls between -128 and +127.

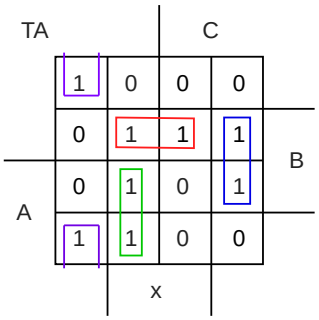
11. (15 points) Construct a 7 to 128 decoder with 3 to 8 decoders with enable. If necessary, configure a 3 to 8 decoder to represent any additional logic needed. Use block diagrams for the components.



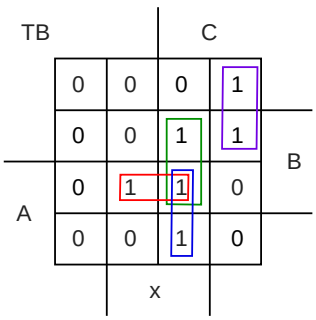
12. (15 points) For the following state diagram.
(a) (5 points) Draw the state table
(b) (4 points) Derive the excitation for implementing this circuit with T flip-flops.
(c) (6 points) Derive the equations for the inputs of the T flip-flops.



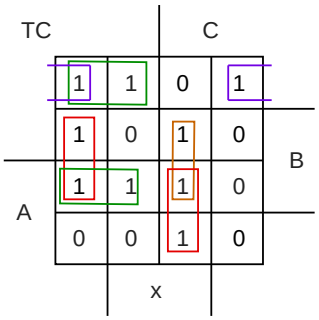
Present State				Next State			Output	FF Inputs		
A	B	C	x	A	B	C		TA	TB	TC
0	0	0	0	1	0	1	0	1	0	1
0	0	0	1	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0	0	0	0
0	1	0	0	0	1	1	0	0	0	1
0	1	0	1	1	1	0	0	1	0	0
0	1	1	0	1	0	1	0	1	1	0
0	1	1	1	1	0	0	1	1	1	1
1	0	0	0	0	0	0	1	1	0	0
1	0	0	1	0	0	0	1	1	0	0
1	0	1	0	1	0	1	0	0	0	0
1	0	1	1	1	1	0	0	0	1	1
1	1	0	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	0	1	1	1
1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	0	1	1



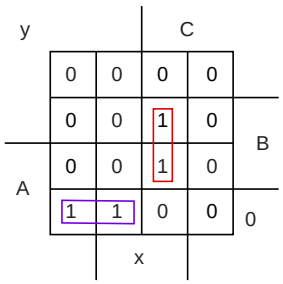
TA = A'Bx + BCx' + AC'x + B'C'x'



TB = A'Cx' + BCx + ABx + ACx

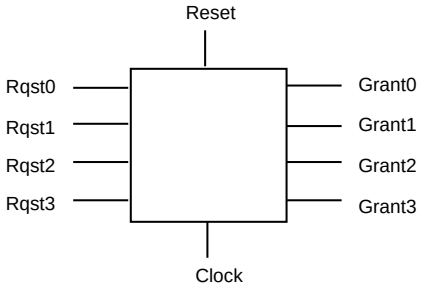


TC = A'B'C' + A'B'x' + BC'x' + BCx + ABC' + ACx



y = AB'C' + BCx

13. (15 points) An arbiter is a circuit that allows at most one subsystem at a time to use a shared resource. A four-way arbiter is shown below. Each subsystem sets its request signal to 1 when it wants to use the resource. When the arbiter sets the grant signal to 1, the subsystem uses the resource. The subsystem sets its request back to 0 when it has finished, and waits for grant to be 0 before starting a subsequent request. While a subsystem is granted use of the resource, other requests must wait, rather than pre-empting the active subsystem. Subsystems are granted requests in order, starting with 0, then 1, 2, 3 and back to 0. A subsystem is skipped if it has no pending request.



Draw a Moore state diagram for this circuit. Do not include the reset in your diagram.