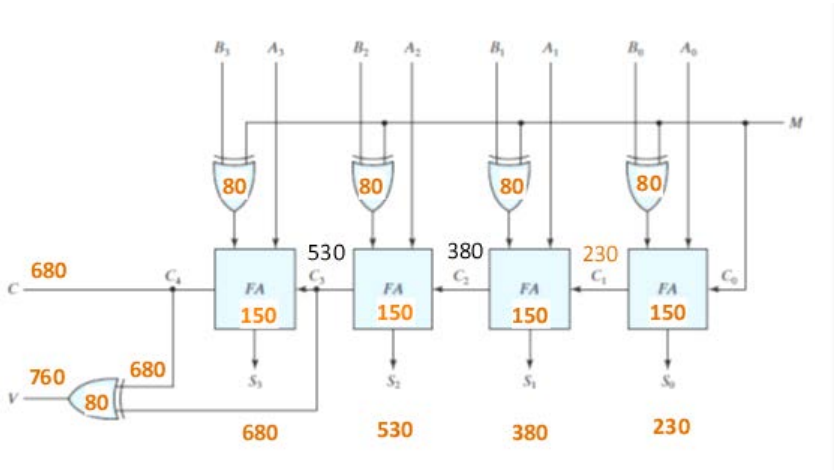
The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Test 2 Solution
Fall 2016

1. (1 point) An _**encoder**_ is a digital circuit that has 2n input lines and n output lines. The output lines generate the binary code corresponding to the input value.
2. (1 point) _**False**_ (True/False) Multiple outputs of a decoder can be 1 at the same time.
3. (1 point)._**True**_ (True/False) Flip-flops exhibit edge sensitive behavior.
4. (1 points) A _Moore_ state machine has outputs that depend only on the state.
5. (1 point) An _**excitation table**__ specifies the flip flop inputs necessary for a present state, next state pair.
6. (15 points) If the delays in the circuit below are as given in the table, find the propagation delays from the inputs to S_0, S_1, S_2, S_3, C and V

Logic Element	Propagation Delay
Inverter	30 ps
AND/NAND	50 ps
OR/NOR	60 ps
XOR	80 ps
Full Adder	150 ps



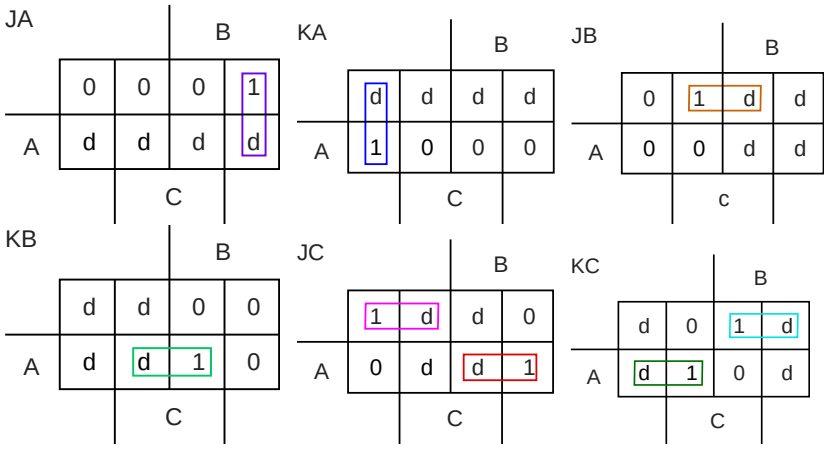
J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

7. (20 points) Design a 3-bit counter which counts in the sequence 000, 001, 011, 010, 110, 111, 101, 100, 000 using clocked JK flip-flops. You do not have to draw the circuit diagram.

Present State			Next State			A		B		C	
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	0	d	0	d	1	d
0	0	1	0	1	1	0	d	1	d	d	0
0	1	0	1	1	0	1	d	d	0	0	d
0	1	1	0	1	0	0	d	d	0	d	1
1	0	0	0	0	0	d	1	0	d	0	d
1	0	1	1	0	0	d	0	0	d	d	1
1	1	0	1	1	1	d	0	d	0	1	d
1	1	1	1	0	1	d	0	d	1	d	0

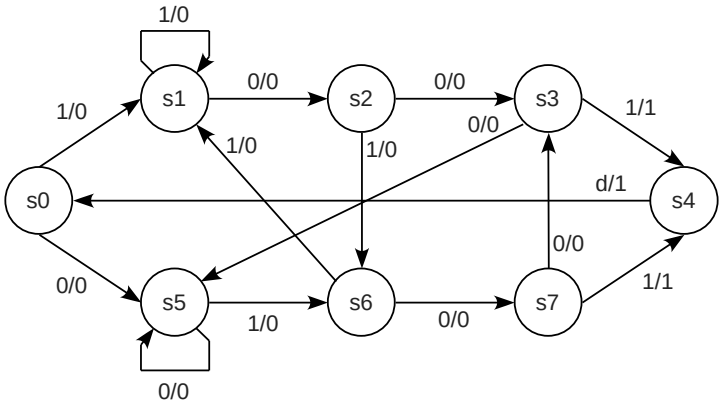


JA = BC', KA = B'C', JB = A'C, KB = AC, JC = A'B' + AB, KC = AB' + A'B

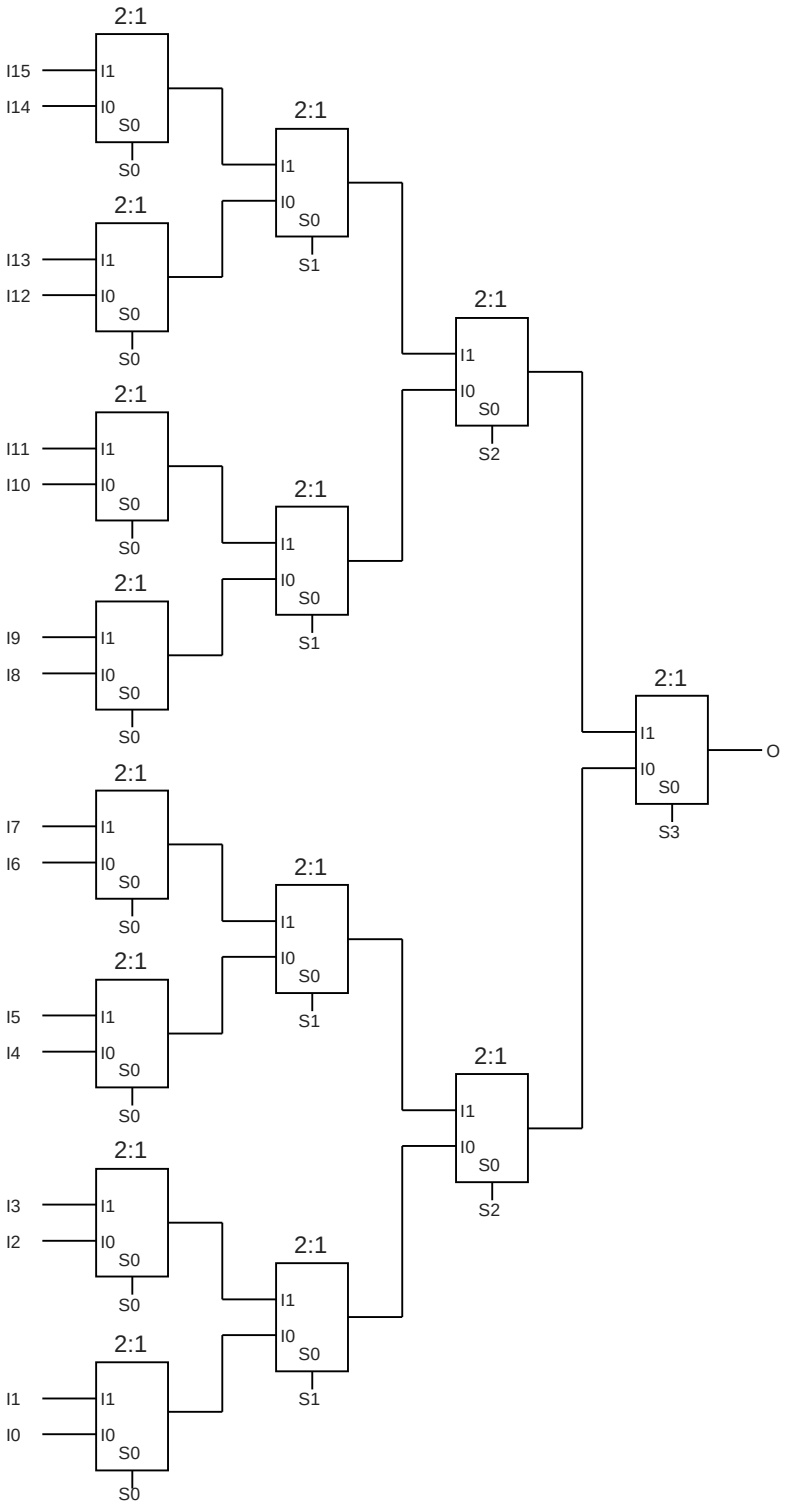
8. (15 points) A synchronous sequential circuit has one input and one output plus a synchronous reset which is active low. If the input sequence 1001 or 0101 occurs, an output of two successive 1s will occur. The first of these 1s should occur coincident with the last input of the 1001 or 0101 sequence. The network should reset when the second 1 output occurs. For example,

Input sequence: 01101100010010 01010 10
Output sequence: 00000000000011 00011 00

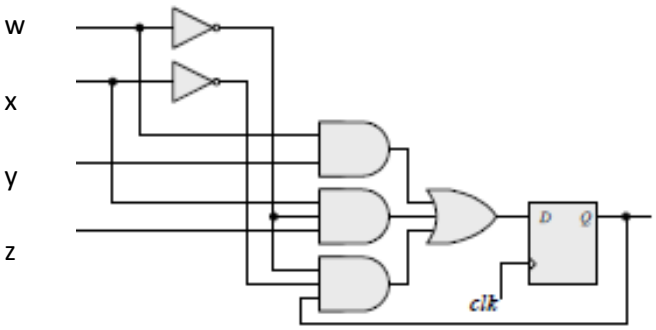
Draw a Mealy state diagram for this circuit. Do not include the reset in your diagram.



9. (15 points) Construct a 16 x 1 multiplexer with as many 2 x 1 multiplexers as you need. Use block diagrams.



10. (15 points) For the figure given, derive the state table.

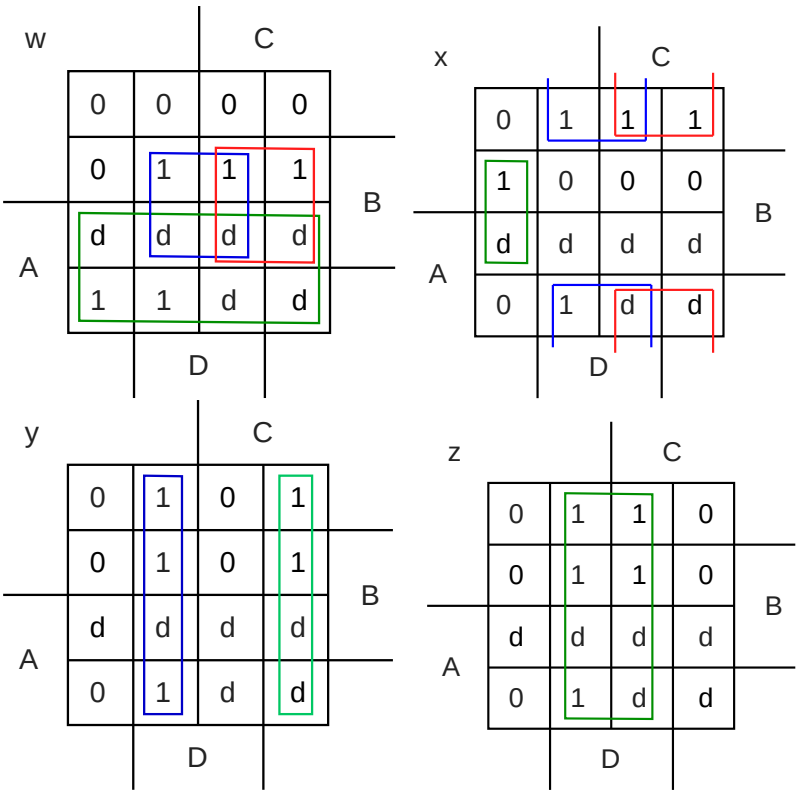


D = wy + w'xz + w'x'A

w	x	y	z	A(t)	A(t+1)
0	0	0	0	0	**0**
0	0	0	0	1	**1**
0	0	0	1	0	**0**
0	0	0	1	1	**1**
0	0	1	0	0	**0**
0	0	1	0	1	**1**
0	0	1	1	0	**0**
0	0	1	1	1	**1**
0	1	0	0	0	**0**
0	1	0	0	1	**0**
0	1	0	1	0	**1**
0	1	0	1	1	**1**
0	1	1	0	0	**0**
0	1	1	0	1	**0**
0	1	1	1	0	**1**
0	1	1	1	1	**1**
1	0	0	0	0	**0**
1	0	0	0	1	**0**
1	0	0	1	0	**0**
1	0	0	1	1	**0**
1	0	1	0	0	**1**
1	0	1	0	1	**1**
1	0	1	1	0	**1**
1	0	1	1	1	**1**
1	1	0	0	0	**0**
1	1	0	0	1	**0**
1	1	0	1	0	**0**
1	1	0	1	1	**0**
1	1	1	0	0	**1**
1	1	1	0	1	**1**
1	1	1	1	0	**1**
1	1	1	1	1	**1**

11. (15 points) Design a code converter that converts a decimal digit from binary coded decimal to the 8, 4, -2, -1 code. You do not need to draw the circuit diagram, equations are good enough.

	BCD				8	4	-2	-1
Number	A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	1	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	0	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	1	1	1
	1	0	1	0	d	d	d	d
	1	0	1	1	d	d	d	d
	1	1	0	0	d	d	d	d
	1	1	0	1	d	d	d	d
	1	1	1	0	d	d	d	d
	1	1	1	1	d	d	d	d



w = A + BC + BD, x = BC'D' + B'C + B'D, y = C'D + CD', z = D