The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Spring 2014
Final Exam Solution

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

1. (1 point)._**0**_ is a controlling value for a NAND gate.
2. (1 point) _**False**_ (True/False) Flip-flops are level sensitive.
3. (1 point) _**True**_ (True/False) When finding the sum-of-products form for a circuit, the procedure is to start with the 1's in a K-map.
4. (1 point) A _**Moore**_ state machine has outputs that depend only on the state.
5. (1 point) A _**register**_ is a group of binary cells.
6. (5 points Convert (64013.25_8) to decimal:

$6 \times 8^4 + 4 \times 8^3 + 0 \times 8^2 + 1 \times 8^1 + 3 \times 8^0 + 2 \times 8^{-1} + 5 \times 8^{-2} =$
$6 \times 4096 + 4 \times 512 + 0 \times 64 + 1 \times 8 + 3 \times 1 + 2 \times 0.125 + 5 \times 0.015625 =$
$24576 + 2048 + 0 + 8 + 3 + 0.25 + 0.078125 = 26{,}635.328125$

7. (10 points) Convert decimal -83 and -62 to binary, using 8-bit signed-2's-complement representation. Then perform the binary equivalent of (-83) + (-62). Convert the answer back to decimal and verify that it is correct or explain why it is not.

$-83 = 1 \times -128 + 0 \times 64 + 1 \times 32 + 0 \times 16 + 1 \times 8 + 1 \times 4 + 0 \times 2 + 1 \times 1 = 1010\ 1101$
$-62 = 1 \times -128 + 1 \times 64 + 0 \times 32 + 0 \times 16 + 0 \times 8 + 0 \times 4 + 1 \times 2 + 0 \times 1 = 1100\ 0010$

-83 1010 1101
-62 1100 0010
0110 1111
$0110\ 1111 = 0 \times -128 + 1 \times 64 + 1 \times 32 + 0 \times 16 + 1 \times 8 + 1 \times 4 + 1 \times 2 + 1 \times 1 =$
$-64 + 32 + 8 + 4 + 2 + 1 = 111$ ×

The result doesn't match because -128 is the most negative number that can be represented in 8-bit signed-2's complement and -83 + -62 = -145. This is an overflow situation.

8. (10 points) How many 4 x 1 multiplexers does it take to construct a 64 x 1 multiplexer?

At the input level, 64/4 = 16 multiplexers are required.
Moving towards the output, the next level requires 16/4 = 4 multiplexers
Still moving towards the output, the next level requires 4/4 = 1 multiplexer
Total = 16 +4 +1 = 21 multiplexers

9. (15 points) A traffic metering system for controlling the release of traffic from an entrance ramp onto a superhighway has the following specifications for a part of its controller. There are three parallel metering lanes, each with its own stop (red) – go (green) light. One of these lanes, the car pool lane, is given priority for a green light over the other two lanes. Otherwise, a "round robin" scheme in which the green lights alternate is used for the other two (left and right) lanes. The part of the controller that determines which light is to be green (rather than red) is to be designed. The specifications for the controller follow:

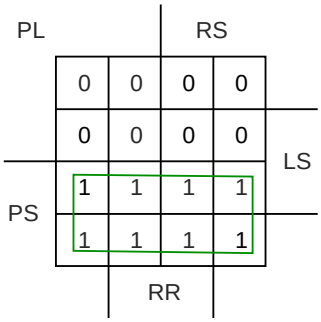
Inputs:
- PS – Car pool lane sensor (car present – 1; car absent – 0)
- LS – Left lane sensor (car present – 1; car absent – 0)
- RS – Right lane sensor (car present – 1; car absent – 0)
- RR – Round robin signal (select left – 1; select right – 0)

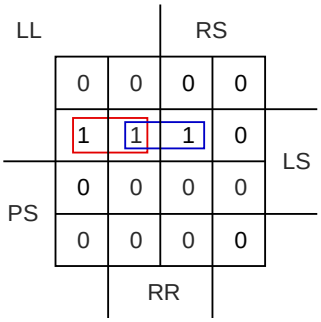
Outputs:
- PL – Car pool lane light (green – 1; red – 0)
- LL – Left lane light (green – 1; red – 0)
- RL – Right lane light (green – 1; red – 0)

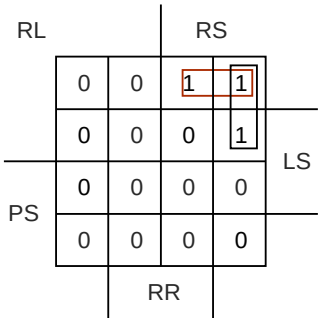
Operation:
1. If there is a car in the car pool lane, PL is 1.
2. If there are no cars in the car pool lane and the right lane, and there is a car in the left lane, LL is 1.
3. If there are no cars in the car pool lane and in the left lane, and there is a car in the right lane, RL is 1.
4. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 1, then LL = 1.
5. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 0, then RL = 1.
6. If any PL, LL, or RL is not specified to be 1 above, then it has value 0.

Design this controller circuit, including developing a truth table, using K-maps to minimize, and drawing a circuit diagram.

PS	LS	RS	RR	PL	LL	RL
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0



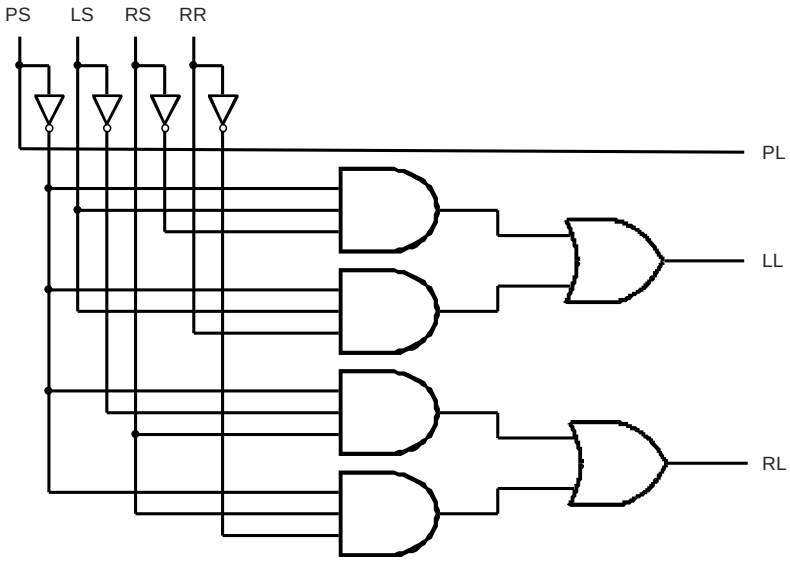




PL = **PS**

LL = **PS' LS RS'** + **PS' LS RR**

RL = **PS' LS' RS** + **PS' RS RR'**



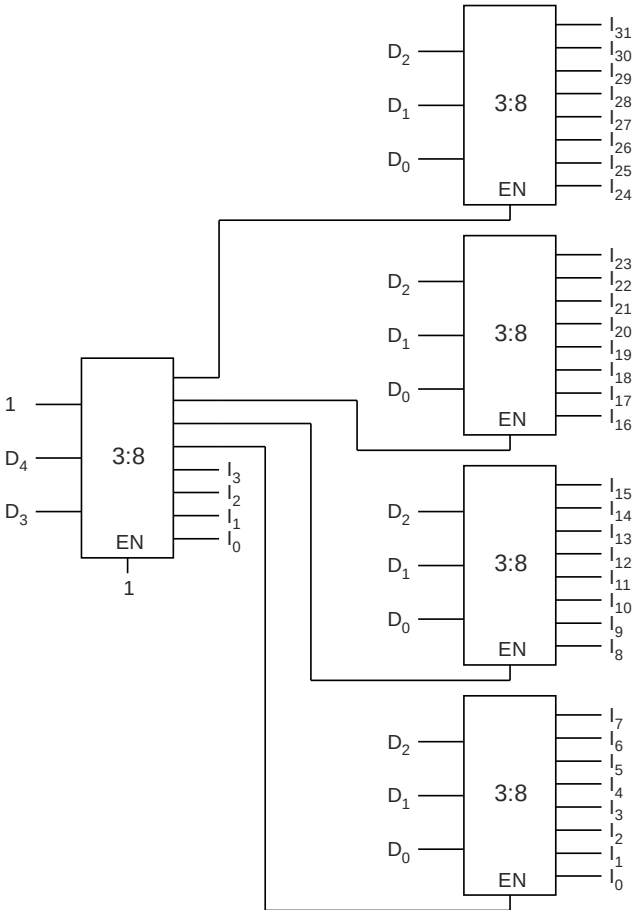
10. (5 points) If a coding system is needed to represent the number of students at UAH (7700), how many bits are required?

 # bits = $\lceil \log_2 7700 \rceil = 13$

11. (5 points) Write out the truth table for a 3-input exclusive-OR gate that has the inputs A, B, and C, and one output, F.

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

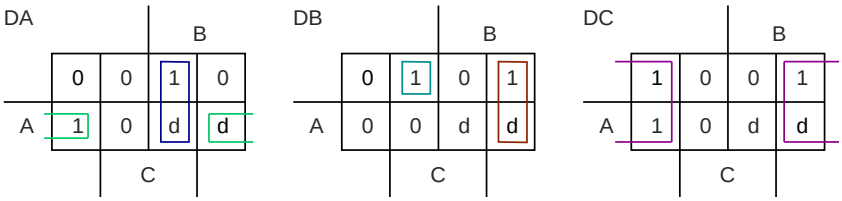
12. (15 points) Construct a 5-to-32 line decoder using only 3-to-8 line decoders with enable. If necessary, configure a 3-to-8 line decoder to represent any additional logic needed. Use block diagrams for the components.



13. (15 points) Design a 3-bit counter which counts in the sequence 000, 001, 010, 011, 100, 101, 000, using clocked D flip-flops. You do not have to draw the circuit diagram. Is the counter self-correcting if it comes up in an unused state?

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State			Next State					
A	B	C	A	B	C	DA	DB	DC
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	0	0	0	0	0	0
1	1	0	d	d	d	d	d	d
1	1	1	d	d	d	d	d	d



DA = AC' + BC DB = A'B'C + BC' DC = C'

Check for self-correcting.

Present State			FF Inputs			Next State		
A	B	C	DA	DB	DC	A	B	C
1	1	0	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0

From 111, the circuit reaches a used state (100) in one cycle. From 110, the circuit reaches a used state in two cycles (100), after having gone through 111.

14. (15 points) A synchronous sequential circuit has one input and one output plus a synchronous reset which is active low. If the input sequence 1001 or 0101 occurs, an output of two successive 1s will occur. The first of these 1s should occur coincident with the last input of the 1001 or 0101 sequence. The network should reset when the second 1 output occurs. For example,

Input sequence: 01101100010010 1101010
Output sequence: 00000000000011 0000011

Draw a Mealy state diagram for this circuit. Do not include the reset in your diagram.