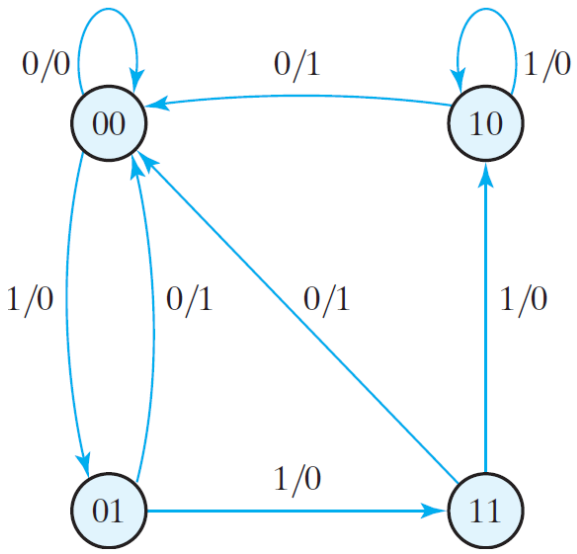
The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Test 2 Solution
Spring 2014

1. (1 point)) A **full adder** is a combinational circuit that forms the arithmetic sum of three bits.
2. (1 point) Unspecified minterms of a function are called **don't care** conditions.
3. (1 point). **False** (True/False) Latches exhibit edge sensitive behavior.
4. (1 point) A **characteristic table** defines the logical properties of a flip-flop by describing its operation in tabular form.
5. (1 point) A **state table** specifies the next state as a function of the present state and inputs.
6. (15 points) Starting from state 00 in the state diagram shown, determine the state transitions and output sequence that will be generated when an input sequence of 00100110011110001 occurs.



Current State	Input	Next State	Output
00	0	**00**	**0**
00	0	**00**	**0**
00	1	**01**	**0**
01	0	**00**	**1**
00	0	**00**	**0**
00	1	**01**	**0**
01	1	**11**	**0**
11	0	**00**	**1**
00	0	**00**	**0**
00	1	**01**	**0**
01	1	**11**	**0**
11	1	**10**	**0**
10	1	**10**	**0**
10	0	**00**	**1**
00	0	**00**	**0**
00	0	**00**	**0**
00	1	**01**	**0**

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

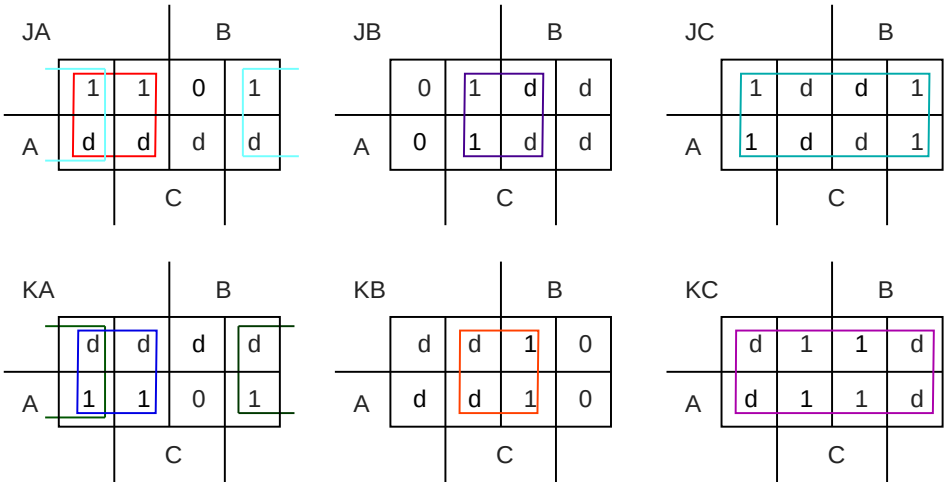
7. (20 points) Design a 3-bit counter which counts in the sequence 000, 101, 010, 111, 100, 001, 110, 011, 000 using clocked JK flip-flops. You do not have to draw the circuit diagram.

Q(t)	Q(t+1)	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

Present State			Next State								
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	1	0	1	1	d	0	d	1	d
1	0	1	0	1	0	d	1	1	d	d	1
0	1	0	1	1	1	1	d	d	0	1	d
1	1	1	1	0	0	d	0	d	1	d	1
1	0	0	0	0	1	d	1	0	d	1	d
0	0	1	1	1	0	1	d	1	d	d	1
1	1	0	0	1	1	d	1	d	0	1	d
0	1	1	0	0	0	0	d	d	1	d	1

JA = B' + C' JB = C JC = 1

KA = C' + B' KB = C KC = 1



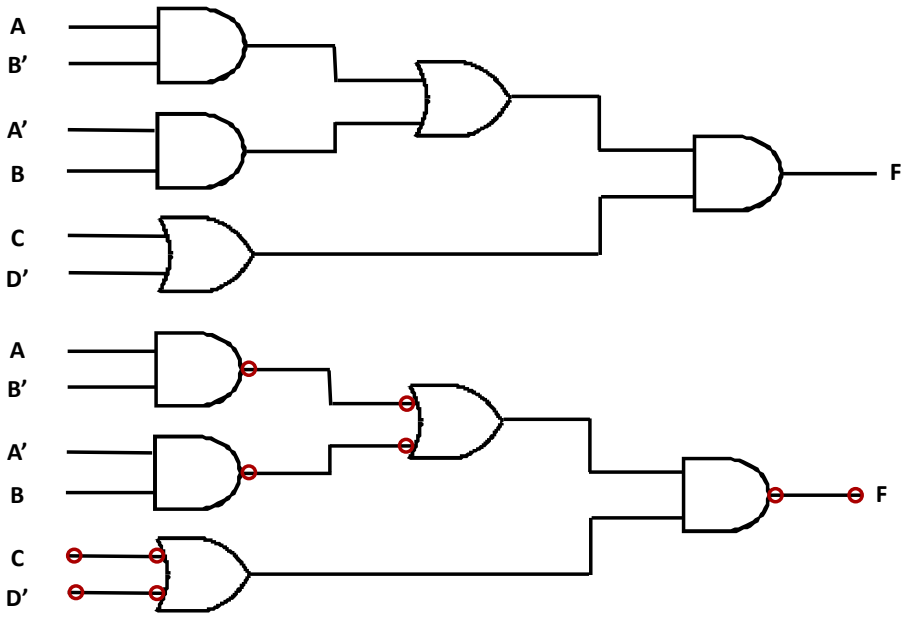
8. (10 points) Reduce the number of states in the following state table, and tabulate the reduced state table:

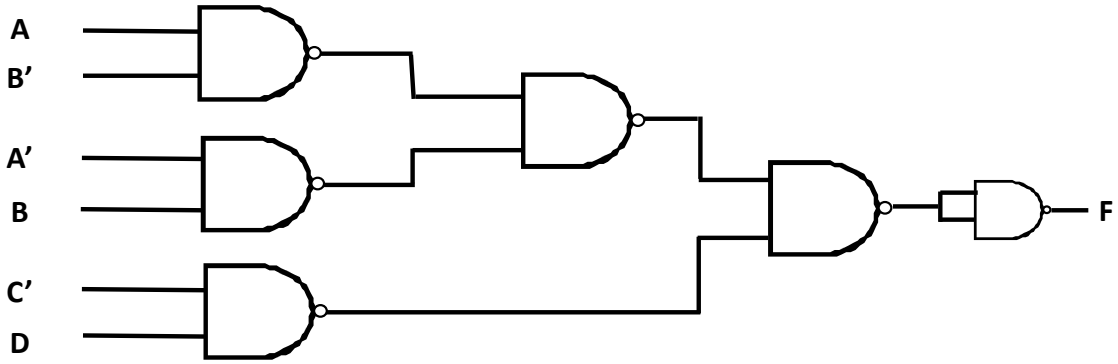
	Next State		Output	
Present State	x = 0	x = 1	x = 0	x = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	1
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

d = h

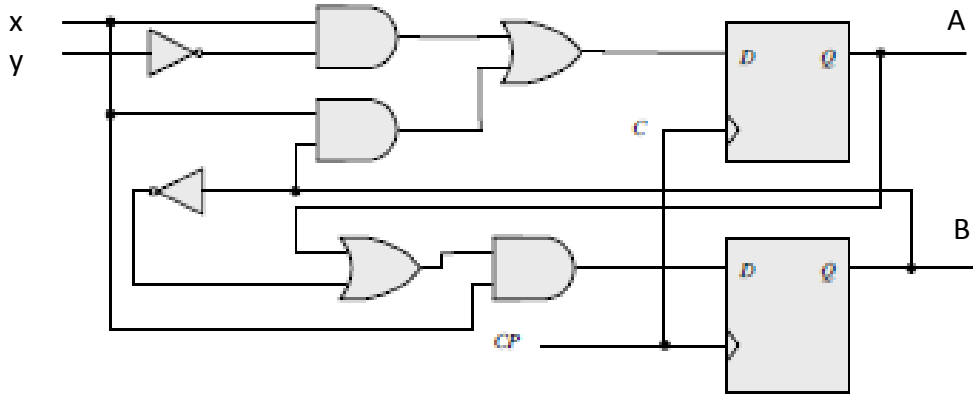
	Next State		Output	
Present State	x = 0	x = 1	x = 0	x = 1
a	**f**	**b**	**0**	**0**
b	**d**	**c**	**0**	**0**
c	**f**	**e**	**0**	**0**
d	**g**	**a**	**1**	**0**
e	**d**	**c**	**0**	**1**
f	**f**	**b**	**1**	**1**
g	**g**	**d**	**0**	**1**

9. (15 points) Convert the following circuit into a circuit that contains only NAND gates.





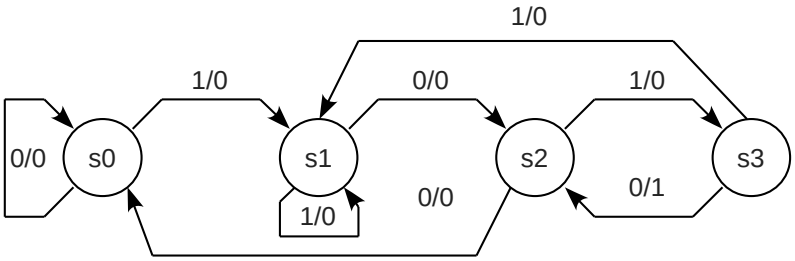
10. (15 points) For the figure given, derive the state table.



x	y	A	B	A(t+1)	B(t+1)
0	0	0	0	**0**	**0**
0	0	0	1	**0**	**0**
0	0	1	0	**0**	**0**
0	0	1	1	**0**	**0**
0	1	0	0	**0**	**0**
0	1	0	1	**0**	**0**
0	1	1	0	**0**	**0**
0	1	1	1	**0**	**0**
1	0	0	0	**1**	**1**
1	0	0	1	**1**	**0**
1	0	1	0	**1**	**1**
1	0	1	1	**1**	**1**
1	1	0	0	**0**	**1**
1	1	0	1	**1**	**0**
1	1	1	0	**0**	**1**
1	1	1	1	**1**	**1**

11. (20 points) Design a Mealy sequential circuit that has an output of 1 whenever its input string has the sequence 1010 and otherwise has an output of 0. These sequences can overlap. Use T flip-flops. You do not have to draw the circuit diagram.

Input: 00101010101000110101 0
Output: 00000101010100000010 1



PS	x	NS	y
S0	0	S0	0
S0	1	S1	0
S1	0	S2	0
S1	1	S1	0
S2	0	S0	0
S2	1	S3	0
S3	0	S2	1
S3	1	S1	0

PS	x	NS	y	TA	TB
00	0	00	0	0	0
00	1	01	0	0	1
01	0	10	0	1	1
01	1	01	0	0	0
10	0	00	0	1	0
10	1	11	0	0	1
11	0	10	1	0	1
11	1	01	0	1	0

TA

A \ B	0	1
0	0	0
1	1	0
1	0	1
0	0	1

x

TB

A \ B	0	1
0	0	1
1	0	1
0	1	0
1	0	1

x

y

A \ B	0	1
0	0	0
1	0	0
0	0	0
0	0	1

x

TA = **AB'x'** + **ABX** + **A'Bx'** TB = **B'x** + **Bx'** y = **ABx'**