The University of Alabama in Huntsville
ECE Department
EE 202 – 01
Spring 2017
Final Exam Solution

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

1. (5 points Convert ($5B2.1A_{12}$) to decimal.

$5 \times 12^2 + 11 \times 12^1 + 2 \times 12^0 + 1 \times 12^{-1} + 10 \times 12^{-2} =$
$5 \times 144 + 11 \times 12 + 2 \times 1 + 1 \times 0.08333 + 10 \times 0.006944 =$
$720 + 132 + 2 + 0.08333 + 0.06944 = 854.1528$

2. (10 points) How many 4 x 1 multiplexers does it take to make a 512 x 1 multiplexer?

First Level **512/4 = 128**
Second Level **128/4 = 32**
Third Level **32/4 = 8**
Fourth Level **8/4 = 2**
Fifth Level **2/4 = 0, but need one, so make 2 to 1 out of 4 to 1**
The total number of multiplexers is 128 + 32 + 8 + 2 + 1 = 171

3. (10 points) Convert decimal +102 and +109 to binary, using 8-bit signed-2's-complement representation. Then perform the binary equivalent of (+102) + (+109). Convert the answer back to decimal and verify that it is correct or explain why it is not.

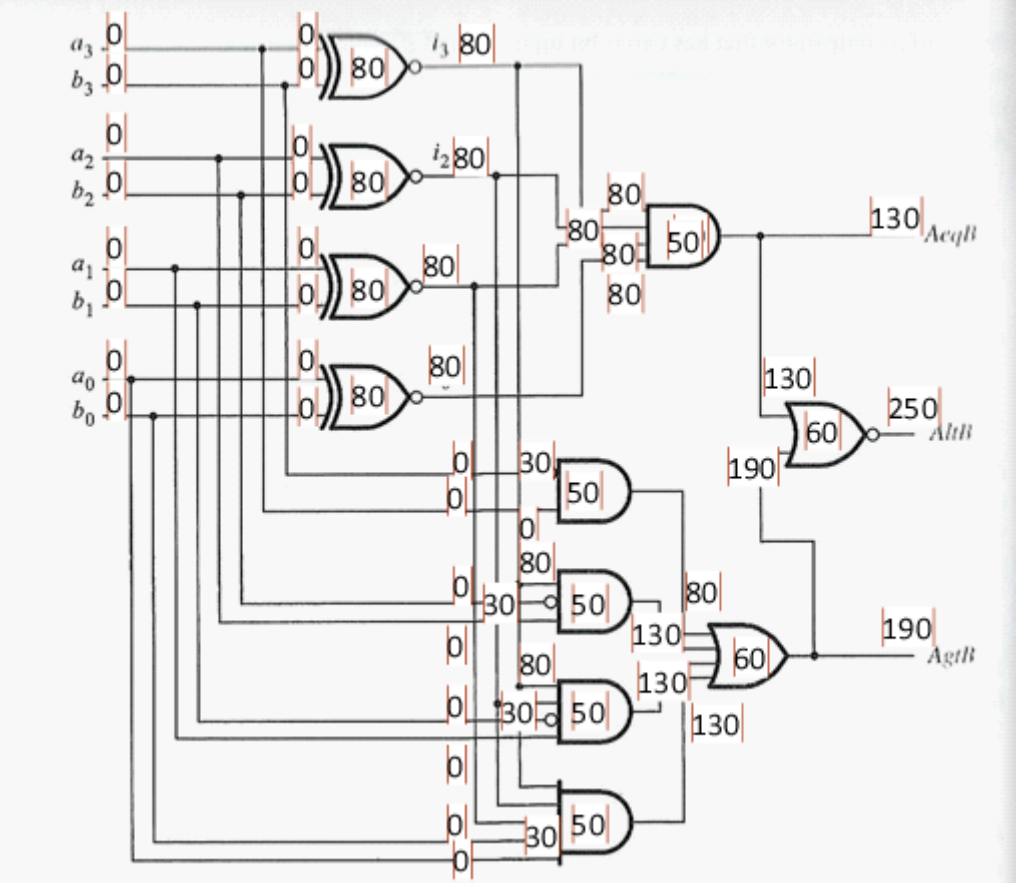
=102 = 0 × -128 + 1 × 64 + 1 × 32 + 0 × 16 + 0 × 8 + 1 × 4 + 1 × 2 + 0 × 1 = 0110 0110
+109 = 0 × -128 + 1 × 64 + 1 × 32 + 0 × 16 + 1 × 8 + 1 × 4 + 0 × 2 + 1 × 1 = 0110 1101

+102 0110 0110
+109 0110 1101
1101 0011
1101 0011 =1 × -128 + 1 × 64 + 0 × 32 + 1 × 16 + 0 × 8 + 0 × 4 + 1 × 2 + 1 × 1 =
-128 + 64 + 16 + 2 + 1 = -45 ✓

The result does not match because 211 does not fall between -128 and +127. This is a case of overflow.

4. (10 points) If the delays in the circuit below are as given in the table, find the propagation delays from the inputs to A < B, A > B, and A = B.

Logic Element	Propagation Delay
Inverter	30 ps
AND/NAND	50 ps
OR/NOR	60 ps
XOR/XNOR	80 ps
Full Adder	150 ps



5 (1 point).A shift register that has bits transferred in one bit per clock cycle is said to have a _**serial**_ load.

6. (1 point) _**ASCII**_ assigns a unique binary representation for specific characters and symbols.

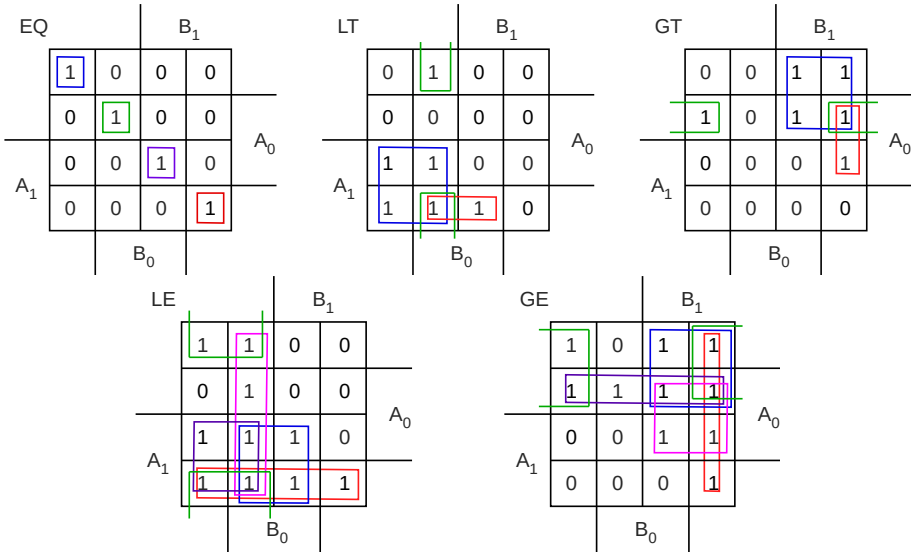
7. (1 point) _**False**_ (True/False) Unsigned numbers can be both positive and negative.

8. (1 point) A _**synchronous**_ counter is one that goes through a predefined set of states when a common clock signal is received at the clock inputs of all flip-flops.

9. (15 points) Consider a circuit that compares two signed two-bit numbers and produces EQ if they are equal, LT if A < B, GT if A > B, LE if A ≤ B, and GE if A ≥ B, as outputs. Derive the equations for the circuitry for EQ, LT, GT, LE, and GE.

A_1	A_0	B_1	B_0	EQ	LT	GT	LE	GE
0	0	0	0	**1**	**0**	**0**	**1**	**1**
0	0	0	1	**0**	**1**	**0**	**1**	**0**
0	0	1	0	**0**	**0**	**1**	**0**	**1**
0	0	1	1	**0**	**0**	**1**	**0**	**1**
0	1	0	0	**0**	**0**	**1**	**0**	**1**
0	1	0	1	**1**	**0**	**0**	**1**	**1**
0	1	1	0	**0**	**0**	**1**	**0**	**1**
0	1	1	1	**0**	**0**	**1**	**0**	**1**
1	0	0	0	**0**	**1**	**0**	**1**	**0**
1	0	0	1	**0**	**1**	**0**	**1**	**0**
1	0	1	0	**1**	**0**	**0**	**1**	**1**
1	0	1	1	**0**	**1**	**0**	**1**	**0**
1	1	0	0	**0**	**1**	**0**	**1**	**0**
1	1	0	1	**0**	**1**	**0**	**1**	**0**
1	1	1	0	**0**	**0**	**1**	**0**	**1**
1	1	1	1	**1**	**0**	**0**	**1**	**1**

A_1A_0 represents the first signed two-bit number and B_1B_0 represents the second signed two-bit number.



EQ = $\mathbf{A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'}$

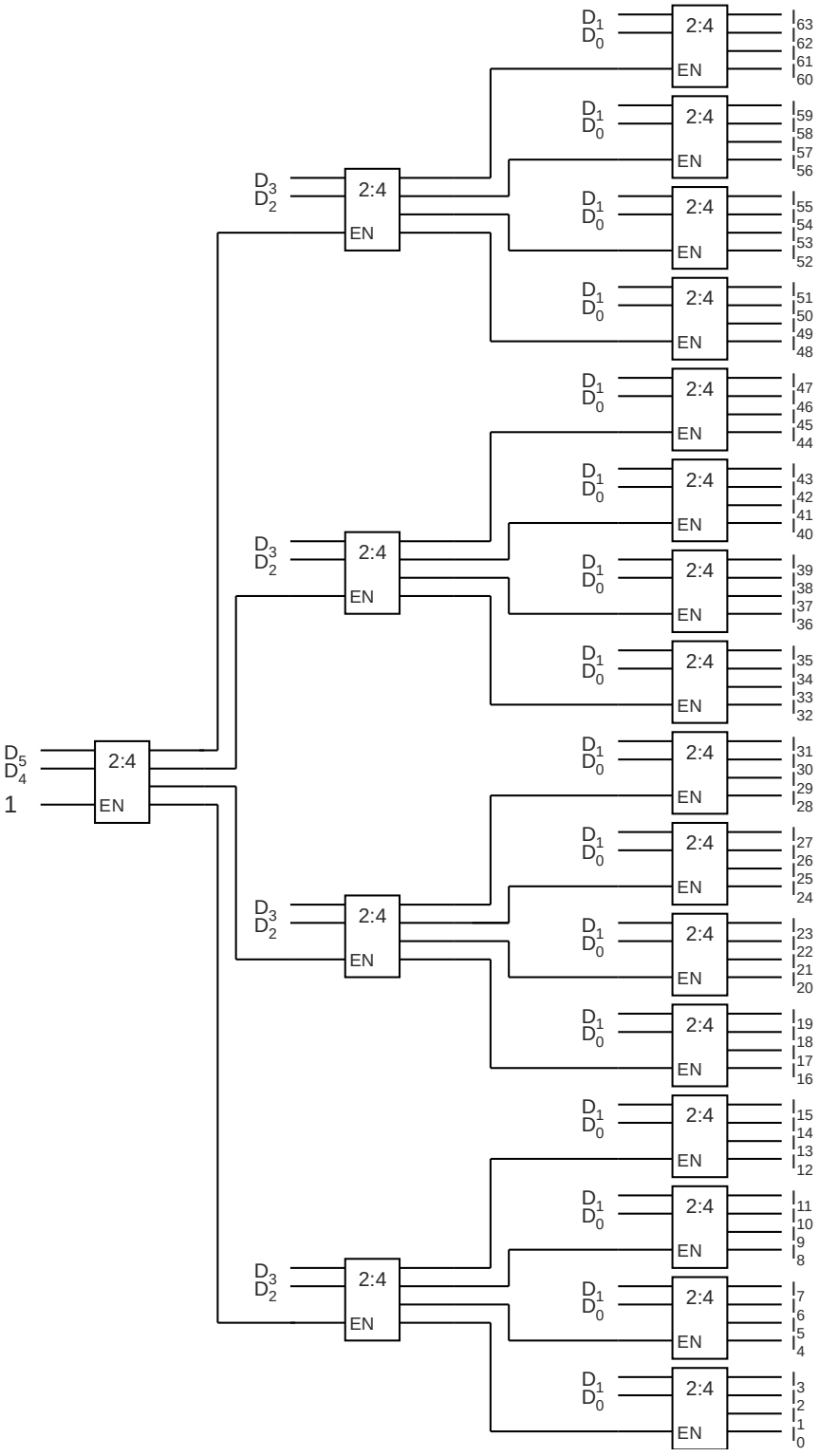
LT = $\mathbf{A_1'B_1' + A_0'B_1'B_0 + A_1A_0'B_0}$

GT = $\mathbf{A_1'B_1 + A_1'A_0B_1' + A_0B_1B_0'}$

LE = $\mathbf{A_1B_0 + A_0'B_1' + A_1A_0' + A_1B_1' + B_1'B_0}$

GE = $\mathbf{A_1'B_1 + A_1'B_0' + B_1B_0' + A_1'A_0 + A_0B_1}$

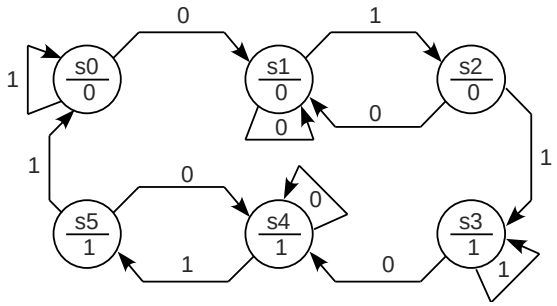
10. (15 points) Construct a 6 to 64decoder with 2 to 4 decoders with enable. If necessary, configure a 3 to 8 decoder to represent any additional logic needed. Use block diagrams for the components.



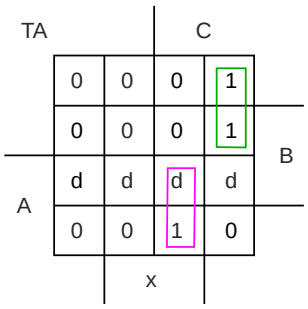
11. (1 point) A **self-correcting** is the name given to a sequential circuit that returns to a valid state after entering an unused state.

12. (15 points) For the following state diagram.

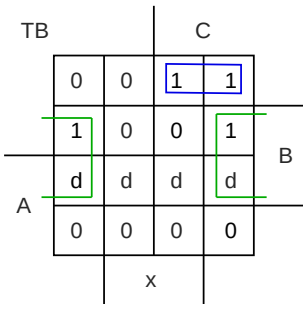
(a) (5 points) Draw the state table
(b) (4 points) Derive the excitation for implementing this circuit with T flip-flops.
(c) (6 points) Derive the equations for the inputs of the T flip-flops and for the output.



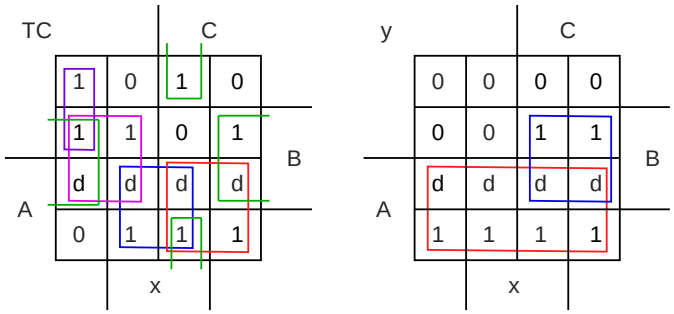
Present State				Next State			Output	FF Inputs		
A	B	C	x	A	B	C	y	TA	TB	TC
0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	1	0	1	1	0
0	0	1	1	0	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0	1	1
0	1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	0	0	1	1	1	1
0	1	1	1	0	1	1	1	0	0	0
1	0	0	0	1	0	0	1	0	0	0
1	0	0	1	1	0	1	1	0	0	1
1	0	1	0	1	0	0	1	0	0	1
1	0	1	1	0	0	0	1	1	0	1
1	1	0	0	d	d	d	0	d	d	d
1	1	0	1	d	d	d	0	d	d	d
1	1	1	0	d	d	d	0	d	d	d
1	1	1	1	d	d	d	0	d	d	d



TA = **A'Cx'** + **ACx**



TB = **Bx'** + **A'B'C**



TC = BC' + Bx' + Ax + AC + A'C'x' + B'CX y = A + BC

13. (15 points) A simple home security system operates as follows.

Inputs: Front gate switch (FS), Motion detector switch (MS)
Asynchronous reset switch (R), Clear switch (C)
Outputs: Front gate melody (FM), Motion detector melody (MM)

- When the R is asserted, the FSM goes to the initialization state (S_init) immediately.
- From state S_init, the FSM unconditionally goes to the wait state (S_wait).
- From state S_wait, the FSM waits for one of the four switches to be activated. All the switches are active-high, so when a switch is pressed or activated, it sends out a 1. The following actions are taken when a switch is pressed:
  1. When FS is pressed, the FSM goes to state S_front. In state S_front, the front gate melody is turned on by setting FM = 1. The FSM remains in state S_front until the clear switch is pressed. Once the clear switch is pressed, the FSM goes back to S_wait.
  2. When MS is activated, the FSM goes to state S_motion. In state S_motion, MM is turned on with a 1. MM will remain on for two more clock periods and then the FSM will go back to S_wait.
  3. From any state, as soon as R is pressed, the FSM immediately goes back to state S_init.
  4. Pressing the clear switch only affects the FSM when it is in state S_front. The clear switch had no effect on the FSM when it is in any other state.

Draw a Moore state diagram of this system that does not include R as an input.