The University of Alabama in Huntsville
ECE Department
EE 202 – 01
Test 2 Solution
Spring 2017

1. (1 point) Storage elements that operate with signal levels (rather than signal transitions) are referred to as _**latches**_
2. (1 point) A _**characteristic table**_ defines the logical properties of a flip-flop by describing its operation in tabular form.
3. (1 point)._**True**_ (True/False) Flip-flops exhibit edge sensitive behavior.
4. (1 points) A _**Moore**_ state machine has outputs that depend only on the state.
5. (1 point) An _**excitation table**_ specifies the flip flop inputs necessary for a present state, next state pair.
6. (15 points) A UAH flip-flop has the characteristic table given. Tabulate the excitation table for a UAH flip-flop.

U	H	Q(t+1)
0	0	1
0	1	Q'(t)
1	0	Q(t)
1	1	0

U	H	Q(t)	Q(t+1)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

UAH Excitation Table

Q(t)	Q(t+1)	U	H
0	0	1	d
0	1	0	d
1	0	d	1
1	1	d	0

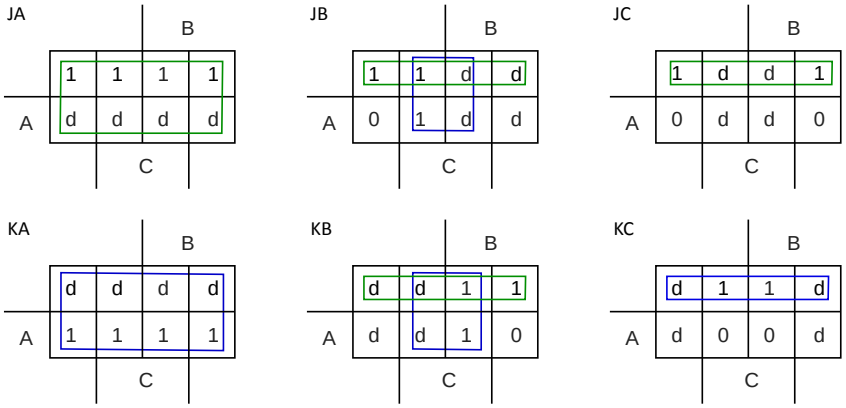
J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

7. (20 points) Design a 3-bit counter which counts in the sequence 000, 111, 001, 110, 010, 101, 011, 100, 000 using clocked JK flip-flops. You do not have to draw the circuit diagram.

Current State			Next State			JA	KA	JB	KB	JC	KC
A	B	C	A	B	C						
0	0	0	1	1	1	1	d	1	d	1	d
0	0	1	1	1	0	1	d	1	d	d	1
0	1	0	1	0	1	1	d	d	1	1	d
0	1	1	1	0	0	1	d	d	1	d	1
1	0	0	0	0	0	d	1	0	d	0	d
1	0	1	0	1	1	d	1	1	d	d	0
1	1	0	0	1	0	d	1	d	0	0	d
1	1	1	0	0	1	d	1	d	1	d	0

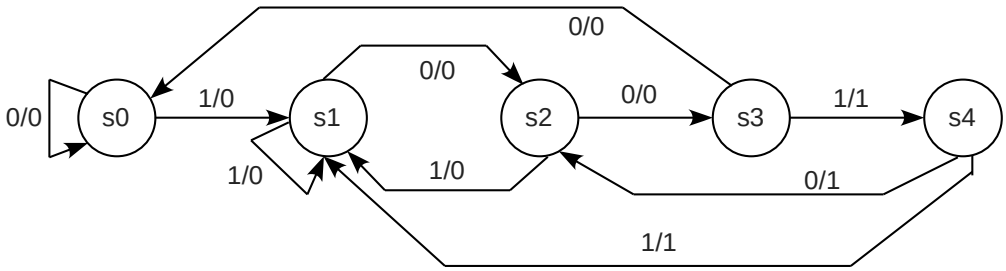


JA = 1, KA = 1 **JB = A' + C, KB = A' + C** **JC = A', KC = A'**

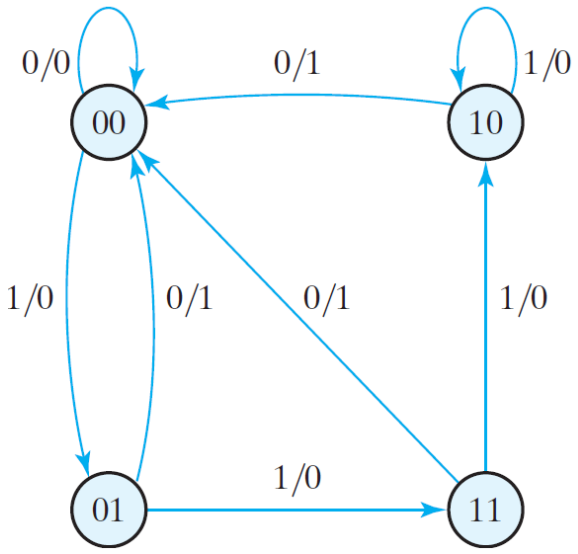
8. (15 points) A synchronous sequential circuit has one input and one output plus a synchronous reset which is active low. If the input sequence 1001 occurs, an output of two successive 1s will occur. The first of these 1s should occur coincident with the last input of the 1001 sequence. Sequences can overlap. For example,

Input sequence: 0110_1110_0100_1001_0101_0
Output sequence: 0000_0000_0110_1101_1000_0

Draw a Mealy state diagram for this circuit. Do not include the reset in your diagram.

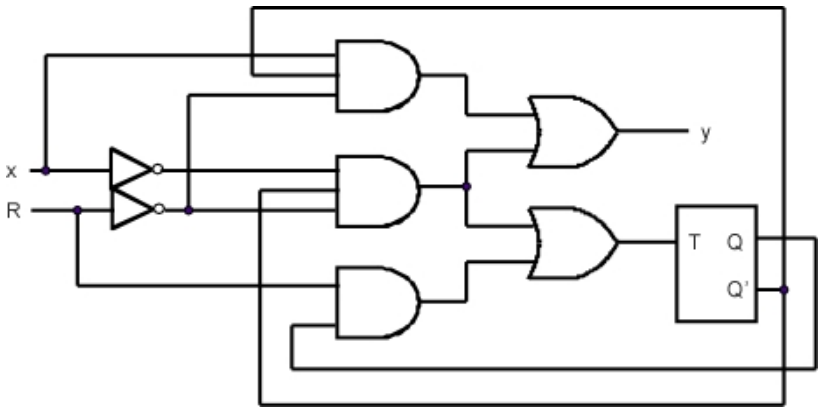


9. (15 points) Starting from state 00 in the state diagram shown, determine the state transitions and output sequence that will be generated when an input sequence of 1110_0101_1011_1100 occurs.



Current State	Input	Next State	Output
00	1	01	0
01	1	11	0
11	1	10	0
10	0	00	1
00	0	00	0
00	1	01	0
01	0	00	1
00	1	01	0
01	1	11	0
11	0	00	1
00	1	01	0
01	1	11	0
11	1	10	0
10	1	10	0
10	0	00	1
00	0	00	0

10. (15 points) For the figure given, derive the state table.

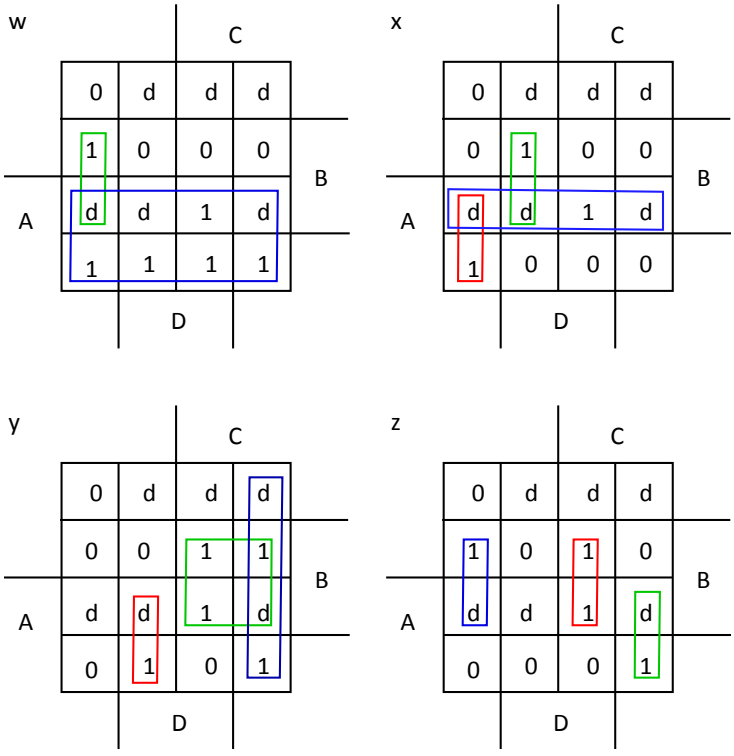


TA = x'R'A' + RA

x	R	A(t)	TA	A(t+1)
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

11. (15 points) Design a code converter that converts a decimal digit from the 8, 4, -2, -1 code to the 5,3,2 -1 code. You do not need to draw the circuit diagram, equations are good enough.

	8	4	-2	-1	5	3	2	-1
Number	A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	1	1
2	0	1	1	0	0	0	1	0
3	0	1	0	1	0	1	0	0
4	0	1	0	0	1	0	0	1
5	1	0	1	1	1	0	0	0
6	1	0	1	0	1	0	1	1
7	1	0	0	1	1	0	1	0
8	1	0	0	0	1	1	0	0
9	1	1	1	1	1	1	1	1
	0	0	0	1	d	d	d	d
	0	0	1	0	d	d	d	d
	0	0	1	1	d	d	d	d
	1	1	0	0	d	d	d	d
	1	1	0	1	d	d	d	d
	1	1	1	0	d	d	d	d



w = A + BC'D' **x = AC'D' + BC'D + AB**

y = AC'D + BC + CD' **z = BC'D' + BCD + ACD'**