

Syllabus: CPE/EE 427, CPE 527

VLSI Design I, Fall 2007

Instructor:	Dr. Aleksandar Milenkovic Office: 217-L	Email: milenka@ece.uah.edu Phone: (256) 824 6830
Office Hours:	Monday 1:00 – 2:00 PM, Wednesday 1:00 – 2:00 PM	
Laboratory Assistant:	Mr. Joel Wilder Phone: (256) 824 3484 Office hours: TBD	Email: wilderj@ece.uah.edu Office: EB 242-C
Time and Place:	Lectures: MW 3:55 PM - 5:15 PM, Engineering Building 239	
Web Page:	http://www.ece.uah.edu/~milenka/cpe527-07F/	
Textbook:	Neil H.E. Weste, David Harris, CMOS VLSI Design: A Circuits and System Perspective, Addison Wesley, 3e, 2005, ISBN: 0-321-14901-7	
Reference Text(s):	1) J. Rabaey, A. Chandrakasan, B. Nikolic, <i>Digital Integrated Circuits: A Design Perspective</i> Prentice Hall, 2/e, ISBN 0-13-090996-3 2) Michael John Sebastian Smith, <i>Application-Specific Integrated Circuits</i> , Addison-Wesley, 1997. ISBN: 0201500221.	
Prerequisites:	EE 202 Introduction to Digital Logic Design, EE 315 Introduction to Electronic Analysis and Design	
Course Description:	The course gives an introduction to digital integrated circuits. It covers the following topics. CMOS devices and manufacturing technology. CMOS inverters and gates. Propagation delay, noise margins, and power dissipation. Sequential circuits, arithmetic, interconnect, and memories. Design methodologies. A major part of the course will be a design project.	
Tentative Schedule:	W1. Introduction into Digital Integrated Circuits, Manufacturing W2. The devices: transistors, resistors, parasitic capacitance W3. CMOS Inverter W4. CMOS Logic, Pass Logic W6. Dynamic view W7. Design for speed, power W8. Sequential Logic Cells, Sequential Logic and Gating W11. Alternative design styles (dynamic, domino, pseudo nMOS) W12. Datapath elements (Adders & Multipliers, Shifters) W14. Class Presentations <i>I reserve the right to change the above schedule based upon the needs of the course.</i>	

Grading Policy: Final course grades will be determined in the manner outlined below:

1	Lab Assignments	15%
2	Homeworks	15%
3	Test I	20%
4	Test II	20%
4	Project	25%
5	Class Participation	5%

Lab Assignments The lab assignments serve two purposes. First, they allow the students to apply what is taught during lectures. After completing all lab assignments the students will have the skills required to complete the main purpose of the lab – the final project. During the first semester the students will design and verify a VLSI circuit using the Cadence / Mentor Graphics CAD tools.

Preliminary Project Info The projects will be done in groups of 2-3 undergraduate (2 graduate) students on the SUN workstations in EB246/216. Project topics are the choice of each design team with the approval of the instructor. Some possible topics include a game; a digital multiply/accumulate/shift unit for a digital filter; an ALU for a CPU; a single chip computer with a limited instruction set; a state machine based score board controller, car/house alarm system; or a shift-register based multiplier. The project will be designed using the CAD tools covered in the lab assignments.

**Tentative
Schedule of
Important Class
Dates** October 10: Test I.
November 26: Test II.
November 19, November 28: Project oral presentations.
December 5: Project written reports due (3:00 PM).
I reserve the right to change the above schedule based upon the needs of the course.

Academic Policies: See course web site: <http://www.ece.uah.edu/~milenka/cpe527-07F/#Info>