CPE/EE 427, CPE 527 VLSI Design I: Homework 1

1. (15 points) Draw a **detailed layout, cross-section and circuit diagram** of a CMOS inverter assuming:
a. (5) Twin-tub process;
**b.** (5) N-well process;
c. (5) P-well process.
Label all relevant regions (n-well, p-well, n+, p+, metal1, poly, ...) and draw connections to Vdd and Gnd. Show transistors as 4-terminal devices.

2. (10 points) Justify the following design rules. Be specific.
a. (2.5) 2λ poly-poly separation;
b. (2.5) no required poly-metal spacing;
c. (2.5) 1λ of diffusion and metal surrounding a cut;
**d.** (2.5) 2λ overhang of poly at transistor gate;

3. (20 points) An NMOS device is plugged into the test configuration shown below. The input Vin =2V. The current source draws a constant current of 50 µA. R is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $k' = 110*10^{-6}$ V/A^2, $V_T = 0.4$, and $V_{DSAT} = 0.6$V. The transistor has a W/L = 2.5µ/0.25µ. For simplicity body effect and channel length modulation can be neglected. i.e $\lambda=0$, $\gamma=0$.

a. (10) When R= 30kΩ again determine the operation region V_D, V_S
b. (10) For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.
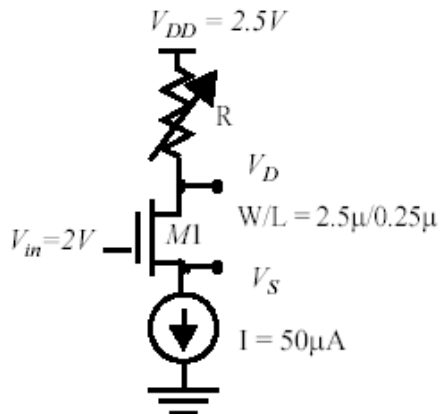
4. (10 points) The circuits below show different implementations of an inverter whose output is connected to a capacitor.

a. (2) Which one of the circuits consumes static power when the input is high?

b. (2) Which one of the above circuits consumes static power when the input is low?

c. (2) V_{OH} of which circuit(s) is 1.2V?

d. (2) V_{OL} of which circuit(s) is 0V?

e. (2) The proper functionality of which circuit(s) depends on the size of devices.
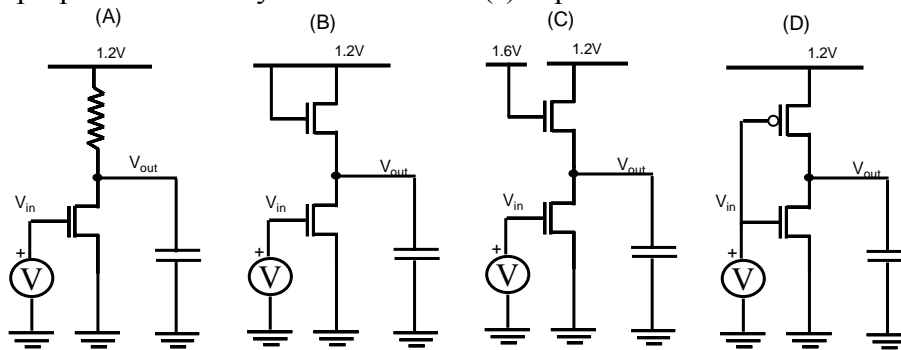
5. (10 points) Textbook: Exercise 2.1.

6. (15 points) Textbook: Exercise 2.2.

7. (10 points) Textbook: Exercise 2.5.

8. (10 points) Textbook: Exercise 2.6.