CPE/EE 427, CPE 527 VLSI Design I: Homework 2

1. (10 points) Complementary CMOS gates
Draw transistor level schematics for the following static complementary CMOS logic cells. Clearly label the inputs (a, b, c, ...), the output (F), Vdd and Gnd. Adjust the sizes of the transistors so that n-channel and p-channel stacks have equal strengths (the same drive strength as a minimum-size CMOS inverter). Assume that logic ratio r=3 (Rpmin/Rnmin). Your implementations should occupy minimal area.

a. (5) A gate that implements the function $\overline{a} \cdot b + a \cdot \overline{b}$. Complements of input signals are not available.

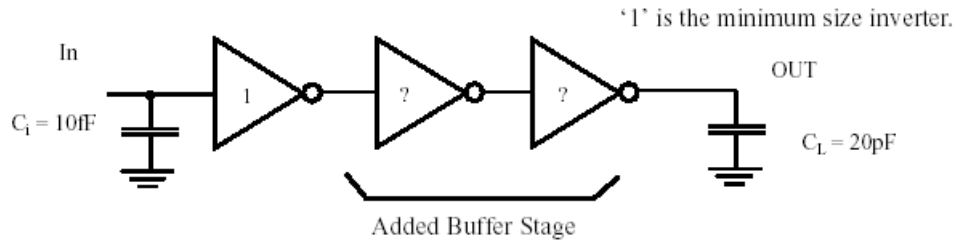
b. (5) A gate that implements the function $\overline{(a+b) \cdot c + d \cdot e \cdot f}$.

2. (20 points) Complementary CMOS.
Draw transistor level schematics for the following complex static CMOS logic cells. Clearly label the inputs, the output, Vdd and Gnd.
a. (5) AOI222
b. (5) AO322
c. (5) OAI311
d. (5) OA33

3. (20 points) Complementary CMOS.
a. (5) Implement the equation (with the minimal number of transistors) X = $((\overline{A}+\overline{B})(\overline{C}+\overline{D}+\overline{E})+\overline{F})\overline{G}$ using complementary CMOS.

b. (5) Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6.
c. (5) Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?
d. (5) Calculate equivalent resistance of the pull-down network when input vector ABCDEFG=1111111.

4. (25 points) Sizing a chain of inverters.
a. (10) In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance Ci = 10fF), you decide to introduce a two-staged buffer as shown in figure below. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.



b. (10) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?
c. (5) Describe the advantages and disadvantages of the methods shown in (a) and (b).

5. (25 points) Logical Effort.
Calculate the path optimum delay and the gate sizes. C_{INV} is the input capacitance of a minimum size inverter. Assume r=2.