CPE/EE 427, CPE 527 VLSI Design I: Homework 3

1	2	3	4	5	[6]	Sum
30	10	25	10	20	30	125

1. (30 points) Misc, Short questions

(a) (2 points) Postponing the introduction of signals with high switching rates (probability of switching close to 50%) can reduce the switching power consumption. **(True | False)**

(b) (2 points) Critical input (the latest arriving input signal) should be connected closest to the GND rail to speed up a complex gate. **(True | False)**

(c) (4 points) Lowering V_{DD} has been widely used to reduce dynamic power consumption. Why?
What are negative effects of lowering V_{DD}?
What is Multi-V_{DD} technique? Is it run-time or design-time technique?

(d) (4 points) How lowering V_T influence the leakage power consumption?

(e) (4 points) What is progressive resizing? Explain.

(f) (4 points) What is charge leakage in dynamic gates? How do we cope with this? Explain.

(g) (2 points) A HI-skew inverter will faster discharge the capacitive load than an unskewed inverter (True | False)

(h) (4 points) What is charge sharing in dynamic gates? How do we cope with this? Explain.

(i) (4 points) What is a threshold drop in pass transistor logic? How do we cope with this? Explain.

2. (10 points) Power consumption

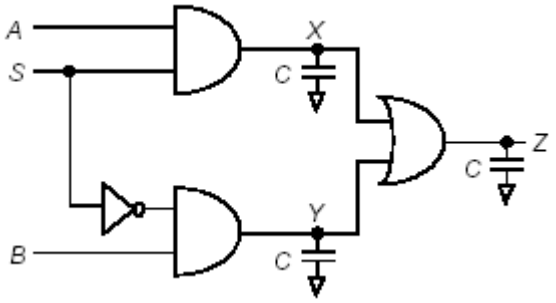
A 180nm standard cell process can have an average switching capacitance C = 150 pF/mm^2. You are synthesizing a chip composed of random logic with an average activity factor of 0.1. Estimate the power consumption of your chip if it has an area of 70 mm^2 and runs at 500 MHz at V_{DD} = 0.9V.

3. (25 points) Power consumption.

Figure below shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs.

a. (5 points) Does this schematic contain reconvergent fan-out? Explain your answer.

b. (10 points) Find the exact signal (P1) and transition ($P_{0 \to ? 1}$) formulas for nodes X, Y, and Z for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation.



c. (10 points) Compute the switching power consumed by the multiplexer, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where C = 0.3 pF. Assume that VDD = 2.5 V and independent, identically-distributed uniform white noise inputs, with events occuring at a frequency of 100 MHz. Perform this calculation for the following: (i) a static, fully-complementary CMOS implementation, (ii) a dynamic CMOS implementation.

4. (10 points) Pseudo-NMOS.

Show transistor schematic of a pseudo nMOS gate that implements the function

$$F = \overline{A(B + C + D) + EFG}$$

5. (20 points) Domino

(a) Give expressions for carry out c_i of each bit of a 4-bit adder (i=1, 2, 3, 4). Use g_i and p_i as inputs ($g_i = a_i$ AND b_i, pi=(a_i XOR b_i). Sketch schematics for carry outs in domino logic.

(b) It is often necessary to compute multiple functions where one is a sub-function of another or shares a sub-function. *Multiple output domino logic* (MODL) combines all the computations into a multiple output gate. Sketch a MODL gate that implements carry c_i of each bit. Discuss advantages and disadvantages of this solution.

6. (30 points) Circuit styles. (Graduate Students Only)
Design a fast 6-input OR gate in each of the following circuit families:
(i) Static CMOS
(ii) Psuedo-NMOS with pMOS transistor ¼ the strength of the pull down stack.
(iii) Domino (a footed dynamic gate followed by Hi-skew inverter); only optimize delay from rising input to rising output.

Sketch an implementation using two stages of logic (e.g., NOR6+INV, NOR3 + NAND2, etc.). Show transistor schematics. Assume that each input can drive no more that 30λof transistor width. The output must drive a 60/30 inverter (pMOS width Wp = 60λ and nMOS width is 30λ). Use logical effort to choose topology and size for least average delay. Estimate this delay using logical effort. When estimating parasitic delays, count only the diffusion capacitance at the output node.