CPE/EE 427, CPE 527 VLSI Design I: Homework 4

1	2	3	4	5	6	7	Sum
15	15	15	15	15	20	15	110

For the following exercises use the timing parameters below.

	Setup Time	Clk-to-Q delay	D-to-Q delay	Contamination delay	Hold delay
Flip-flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

1. (15 points) Propagation delay
For each of the following sequencing styles, determine the maximum logic propagation delay available within a 500 ps clock cycle. Assume there is zero clock skew and no time borrowing takes place.
(a) Flip-flops
(b) Two-phase transparent latches
(c) Pulsed latches with 80 ps pulse width.

2. (15 points) Repeat the exercise 1 if the clock skew between any two elements can be up to 50 ps.

3. (15 points) Contamination delay
For each of the following sequencing styles, determine the minimum logic contamination delay in each clock cycle (or half-cycle for two-phase latches). Assume a zero clock skew.
(a) Flip-flops
(b) Two-phase transparent latches with 50% duty cycle clocks
(c) Two-phase transparent latches with 60 ps of nonoverlap between phases
(d) Pulsed latches with 80 ps pulse width.

4. (15 points) Repeat the exercise 3 if the clock skew between any two elements can be up to 50 ps.

5. (15 points) Time borrowing
Suppose one cycle of logic is particularly critical and the next cycle is nearly empty. Determine the maximum amount of time the first cycle can borrow into the second for each of the following sequencing styles. Assume there is zero clock skew.
(a) Flip-flops
(b) Two-phase transparent latches with 50% duty cycle clocks
(c) Two-phase transparent latches with 60 ps of nonoverlap between phases
(d) Pulsed latches with 80 ps pulse width.

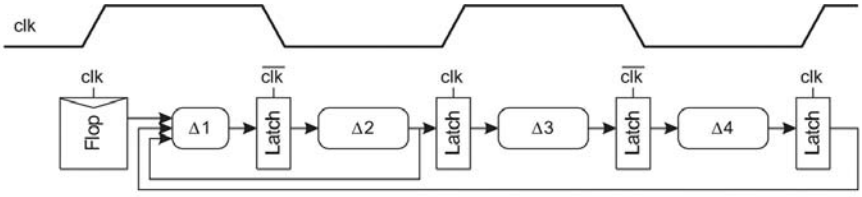
6. (20 points)

Determine the minimum clock period at which the circuit below will operate correctly for each of the following logic delays. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay Δ's.

(a) Δ1 = 300 ps, Δ2 = 400 ps, Δ3 = 200 ps, Δ4 = 350 ps.

(b) Δ1 = 300 ps, Δ2 = 400 ps, Δ3 = 400 ps, Δ4 = 550 ps.

(c) Δ1 = 300 ps, Δ2 = 900 ps, Δ3 = 200 ps, Δ4 = 350 ps.



7. (15 points) FF design

Consider the following edge-triggered register. Assume that the clock inputs CLK and CLK have a 0V to V_{DD} swing. Also assume that there is no skew between CLK and CLK (i.e., the inverter delay to derive CLK from CLK is zero). Assume that the rise/fall times on all signals are zero.

(a) (5 points) What type of register is this? Explain. (Positive Edge-Triggered Register or Negative Edge-Triggered Register).

(b) (10 points) Assume that the propagation delay of each clocked inverter (e.g., M_1-M_4) is $T_{CK\text{-}INV}$ and the delay of inverters I1 and I2 is T_{INV}. Derive the expression for the set-up time (t_{SU}), the propagation delay ($t_{c\text{-}q}$) and the hold time (t_h) in terms of the above parameters, $T_{CK\text{-}INV}$ and T_{INV}.