CPE/EE 427, CPE 527, VLSI Design I:
Tutorial #2, Schematic Capture, DC Analysis, Transient Analysis (Inverter, NAND2)

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1. INTRODUCTION

In this tutorial exercise you will learn how to use Cadence's schematic capture tool to create an inverter and then simulate it. You will build the inverter in the schematic tool at the circuit level and will construct a symbol in which to package your inverter design. Next, you will instantiate your inverter symbol into a "test workbench" file, where you will do a spice simulation using Spectre to analyze the transient and DC characteristics of your design. Subsequently, you will do a post-layout simulation that will use the inverter layout from tutorial 1, where the parasitic capacitances are extracted and incorporated into the simulation. Finally, using this workflow as a guide, you will create a two-input static NAND gate on your own and simulate it using Spectre.

You will base your MOSFETs on the TSMC 0.25um 5-metal 2.5V process that was used for Tutorial 1 (MOSIS SCN5M_DEEP).

2. CADENCE STARTUP

From your home directory, change directories into your cadence working directory:

$ cd cadence

$ cd lab1_2

Start the cadence tool:

$ icfb&

3. CREATE DESIGN WORK AREA

In the Library Manager window, select TestLib, the library you created in tutorial 1.

Select the MyINV cell and add a new cell view (as was done in tutorial 1). Ensure the name of the new cell view is MyINV and make sure you select "**Composer-Schematic"** in the Tool pulldown window. Click OK, and the Schematic tool will open, as shown in Figure 1.

Figure 1. Schematic Capture Tool.

4. CREATE INVERTER CIRCUIT

The schematic capture tool will be used to draw the schematic representation of your inverter.

To draw the inverter you need to add a pmos4 transistor, nmos4 transistor, ground connection, power supply connection, input pin, output pin, and wire it together.

To add items to your schematic, go to **Add->Instance** in the composer tool, or press the letter 'i' (or select the icon pictured on the left vertical toolbar). The add instance pop-up appears like in Figure 2. Click on browse to graphically get components, where you will see the window as shown in Figure 3.
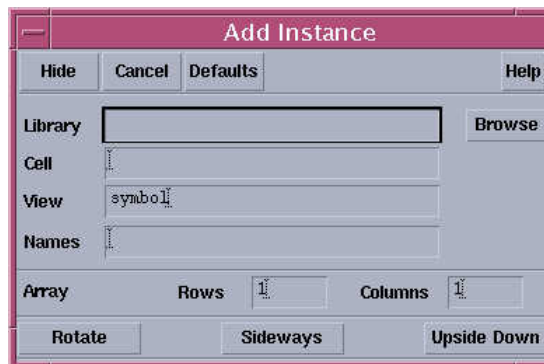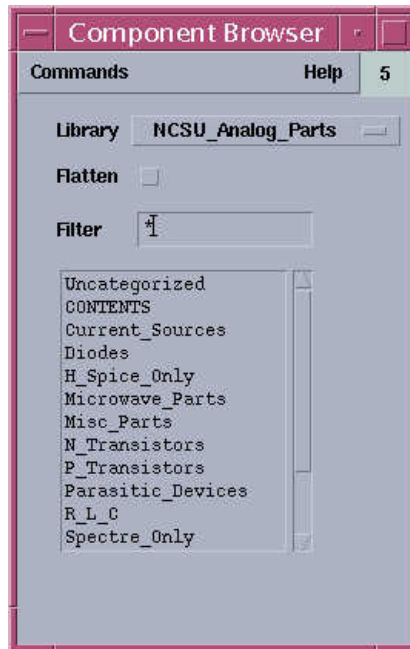

Figure 2. Adding an instance.

Figure 3. Browsing for components.

To get the parts, make sure the library is set to NCSU_Analog_Parts.

In the component browser window, click on supply nets and select vdd. (The items in supply nets are actually global signals, which are automatically given pins. This makes symbols cleaner because only logic ports are designated.)

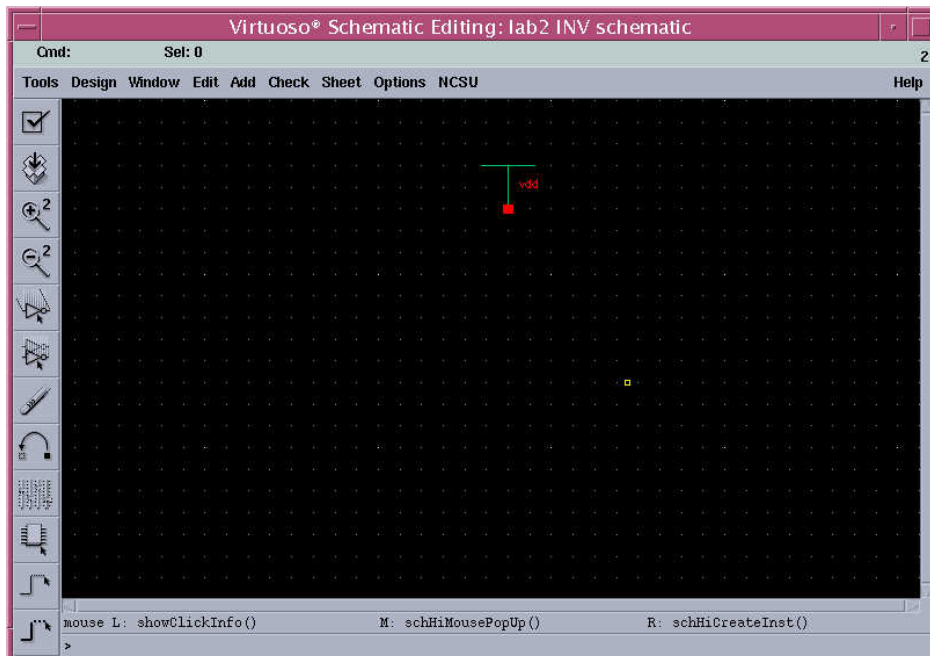Stamp down the vdd instance in your schematic like in Figure 4.

Figure 4. Stamping down vdd.

Get the gnd symbol and stamp it down in the same manner as you did for vdd.

To add the transistors, click on N_Transistors for the nmos4 and P_Transistors for the pmos4. Add an nmos4 and a pmos4 transistor in a similar manner. The pop-up for the nmos4 should look like Figure 5, and the pmos4 pop-up should look like Figure 6**.**

Make the W/L ratio for your nmos4 4λ/2λ, and make the W/L ratio for your pmos4 8λ/2λ. *(NOTE: If your transistor does not have the widths and lengths like in Figure 5, you did not attach a tech library to the library you created for tutorial 2 and you will need to start over.)*

Stamp them down like Figure 7. It does not have to be exact but neatness will make the design easier to work with. (If you make a mistake and need to get out of add instance mode, press the esc key. Click on the object you want to delete and press the del key.)
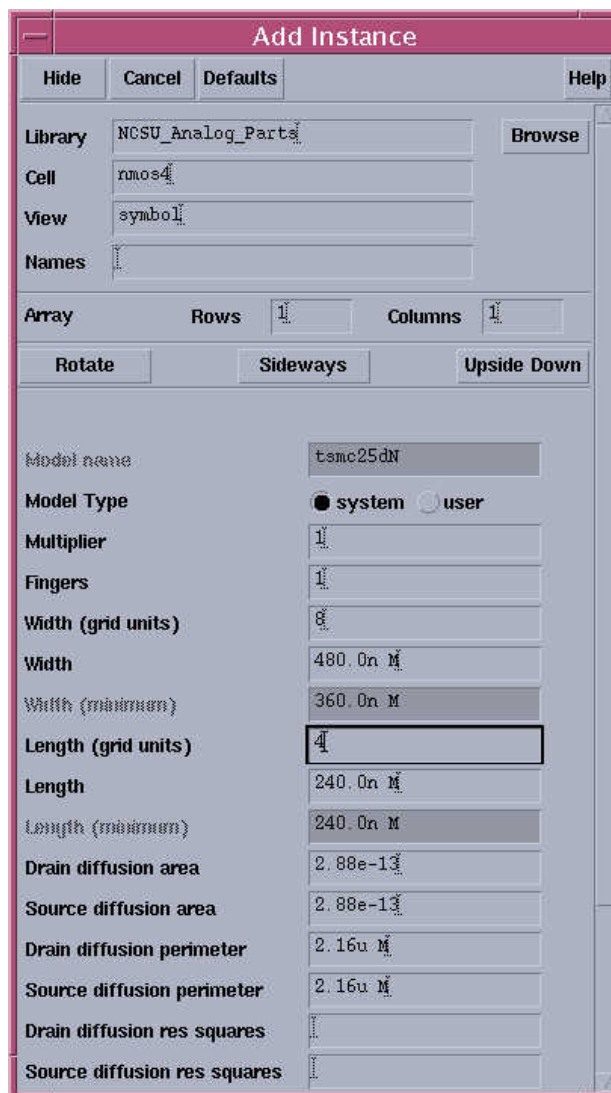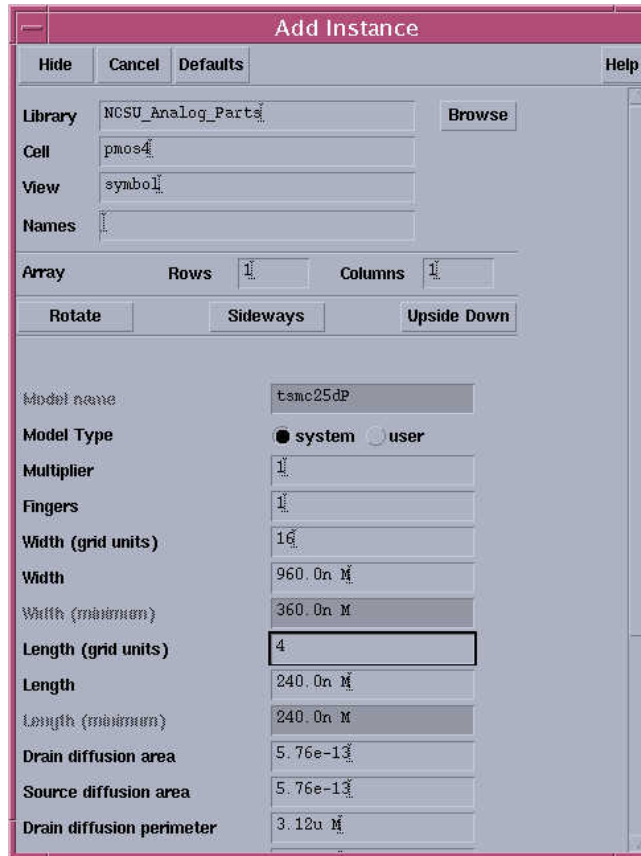

Figure 5. Getting an nmos4 device.

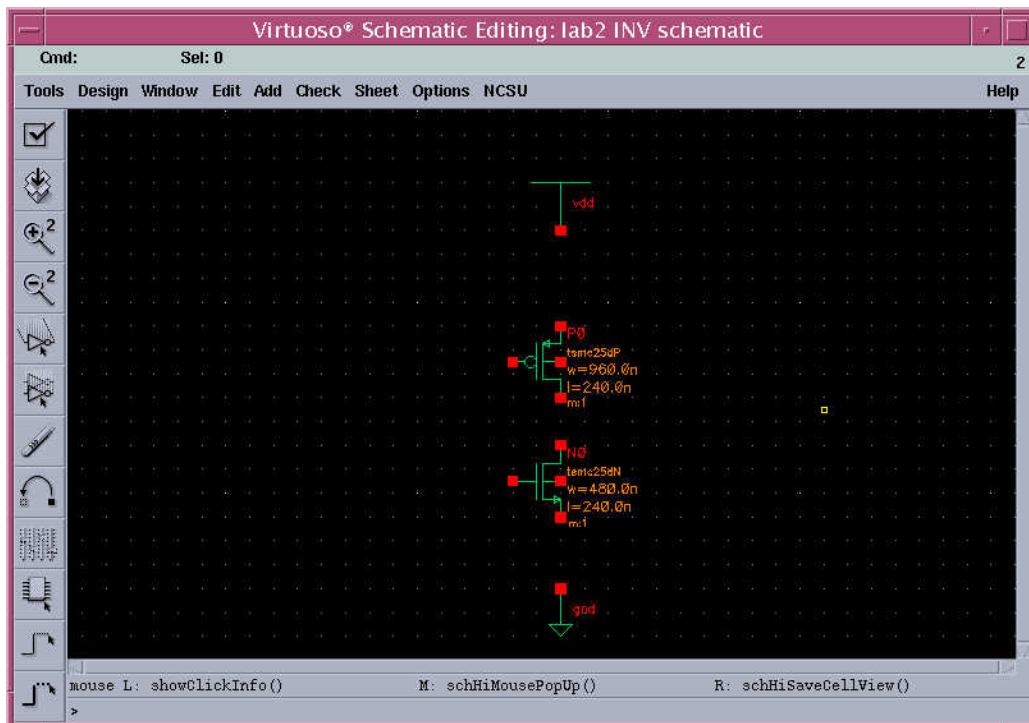Figure 6. Getting a pmos4 device.

Figure 7. Major symbols of the CMOS inverter.

All that remains to be completed is to wire the connections together and add input and output pins. To add a wire, press w. The wire will snap to place at the proper ports of each device by pressing the 's' key near that node.
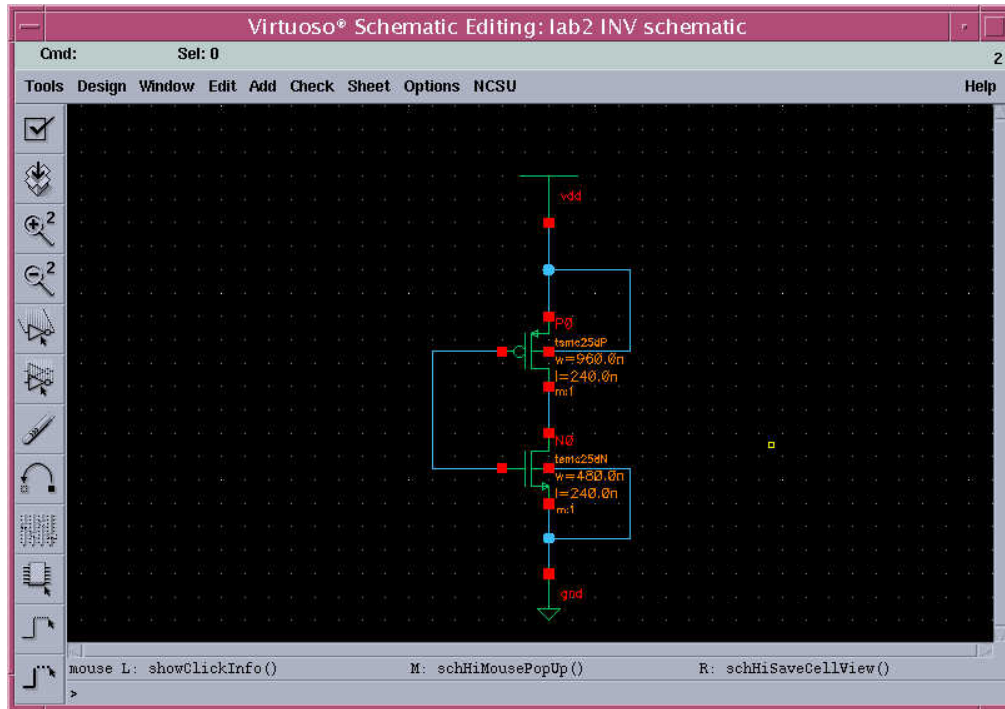Wire it up like Figure 8.

Figure 8. Wiring a CMOS inverter.

To add the input and output pins, go to **Add->pins** and a pop up like Figure 9 should appear. Fill it out exactly like Figure 9. The pin names must match the pin names of the symbol view you are going to create later**.** If they do not match (direction or name), the design, check & save routine will fail.
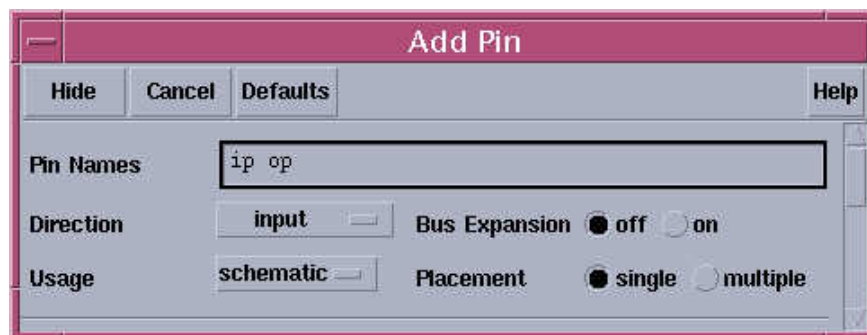

Figure 9. Add pin pop-up.

Stamp down the input pin like in Figure 10.
Change the direction of the Y pin in the add pin pop-up to output.
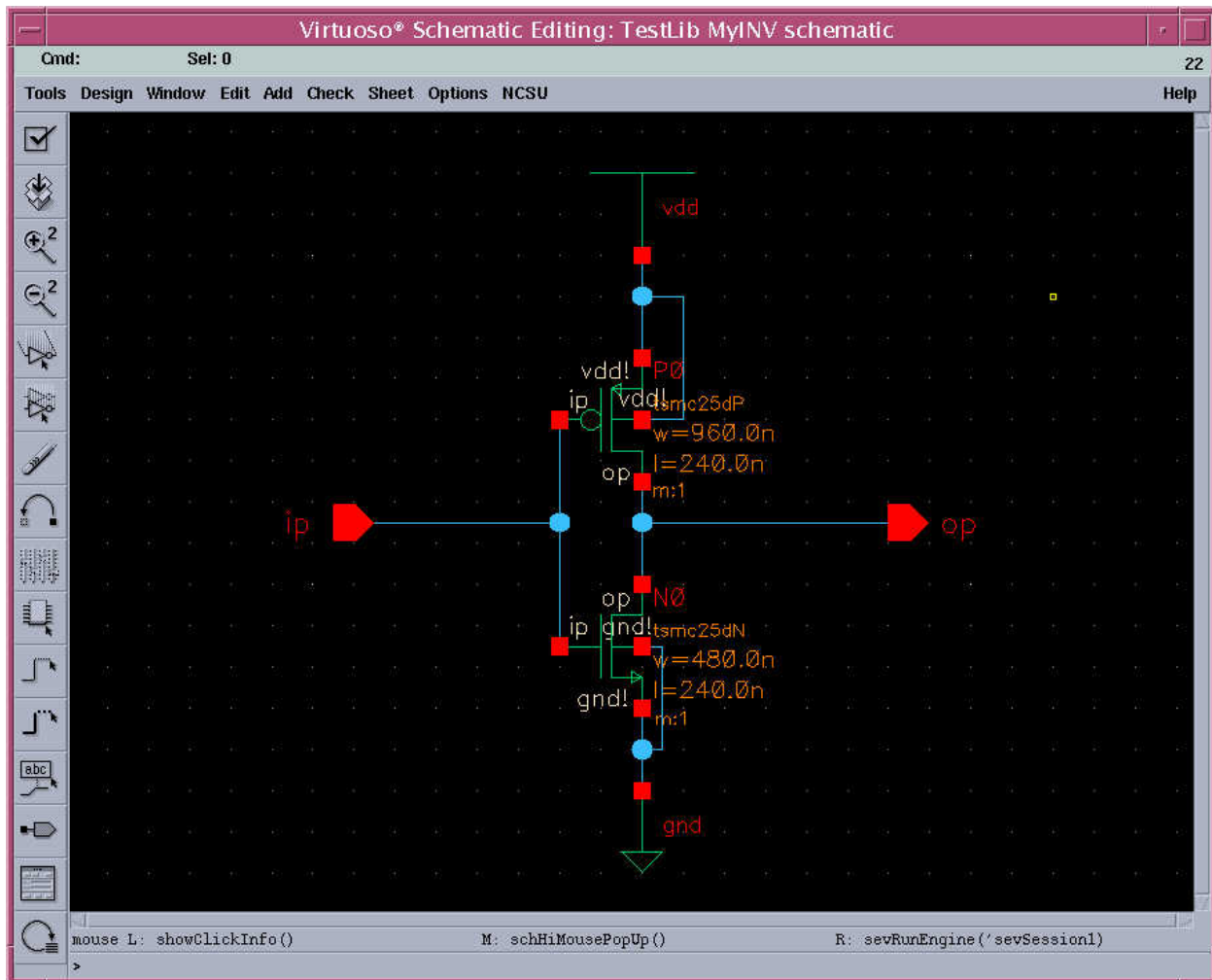Stamp it down like in Figure 10.

Figure 10. Completed schematic.

To connect the substrate of the pmos transistor to vdd, press the esc key to get out of the add pin mode and then press w to enter the wire mode. While in wire mode connect the nmos substrate to ground as well.

To save and check your schematic for errors, go to **Design->Check & Save.** Any errors will be highlighted in the schematic window. (The CIW window will let you know the results of the schematic check.) You can exit the schematic capture tool at this time (go to **Window->Close**).

5. CREATE INVERTER SYMBOL

To use a test bench (test bench means a separate schematic where you will connect voltage sources and whatever else for simulating your design) you must have a symbol view of the inverter. Do not use this inverter's schematic view as a test bench; otherwise, it will not pass LVS (LVS means layout versus schematic).

To create a symbol view:
1. Go to the Library Manager window and create a new cell view in your current working library for lab2. When the window appears for creating the new cell, select the "Composer-Symbol" tool from the pulldown window and make sure the cell name is the same as the previously

created inverter schematic cell. Click OK and the symbol editor window will appear, as shown in Figure 11.
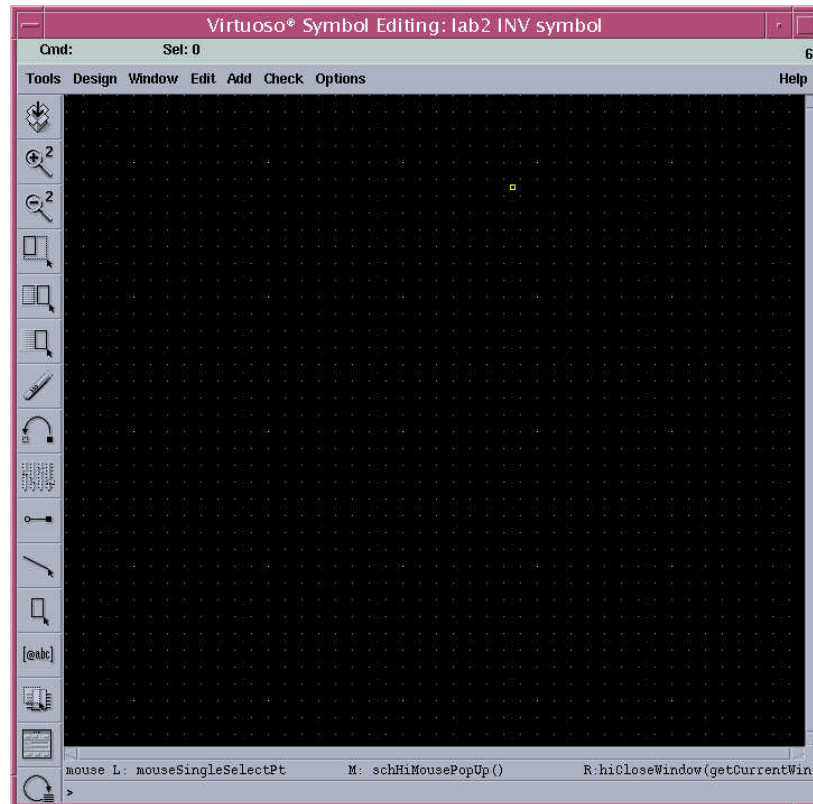

Figure 11. Symbol editor.

The symbol editor allows you to draw any kind of shape to represent your logic gate. The important part is to have the input and output pins match whatever it is you are representing. In this case, you need to match the input pin A and output pin Y of the inverter. Rather than drawing an inverter symbol from scratch, it is much easier to copy one that has already been drawn.

To import a symbol:
1. Go to **Add->import symbol** and a pop-up window will appear. Click on browse and select the inverter in the digital library of the NCSU kit (NCSU_Digital_Parts->inv->symbol).
2. Stamp the symbol down into the symbol editor, as shown in Figure 12. (note that the names of the pins will need to be changed so that they match the names that were assigned to the inverter in the schematic cell)
3. Press the esc key to get out of add symbol mode.
4. Press the f key to fit the symbol in your window.
5. For each of the pin names, do the following:
      1.   Select the actual pin (the red square), press 'q', and change the 'A' ('Y') to 'ip' ('op')
      2.   Select the text label, press 'q', and change the 'A' ('Y') to 'ip' ('op')
6. Go to **Design->check & save**. You should have no errors (check the CIW window). If there are errors, the pins must be wrong in your schematic. Go back to your schematic and fix the pin assignments. Also, check for direction and name. If there is one pin misnamed, you will see the following two errors:
      1. A pin in the schematic view was not found in the symbol view.

2. A pin in the symbolic view was not found in the schematic view.
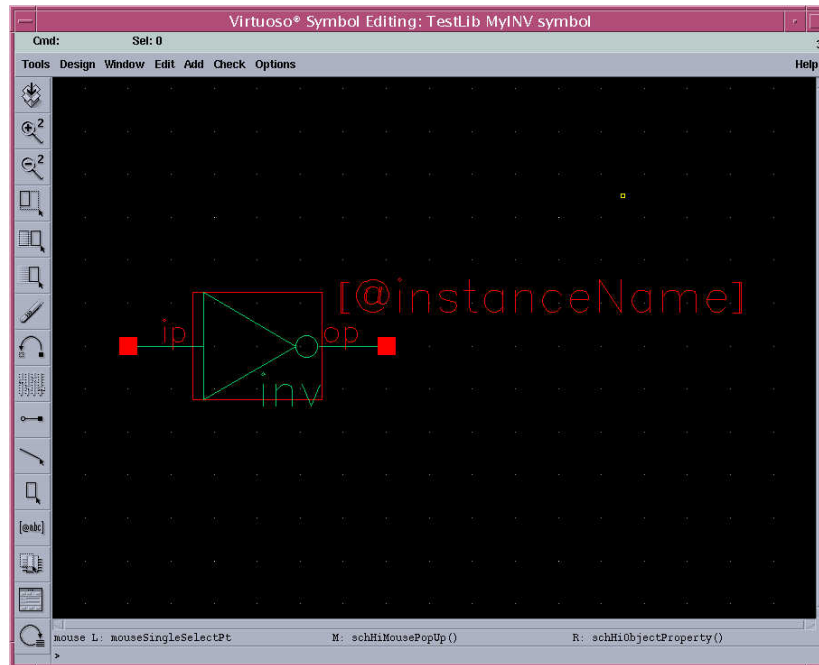

Figure 12. The inverter's symbol.

Close the symbol editor by going to **Window->Close**.

6. CREATE INVERTER TEST BENCH

Now that you have created a schematic and symbolic view of your inverter, it is time to create a test bench. This will be a virtual test bench, but it will have to have a power supply, input vectors, and a ground (plus the inverter) to test its transient response and DC response.

To create the inverter test bench:

In the Library Manager, go to **File->New->Cell view**. Create a new cell in your lab2 library and name it INV_TB, and assign this cell to the Composer-Schematic tool.

In the schematic editor press 'i' or go to **Add->Instance**. (This is the same way you added the pmos4 and nmos4 previously in your inverter schematic.) Click on browse, and this time select your lab2 library. Click on flatten and select your inverter (this is the symbol that you just created). Stamp it down in your schematic.

While still in add instance mode, add the **gnd** and **vdd** global symbols just like you did when creating the schematic for your inverter. Add the power supply (vdc from voltage sources in NCSU_Analog_Parts) and set the DC voltage to 2.5 Volts, as shown in Figure 13.
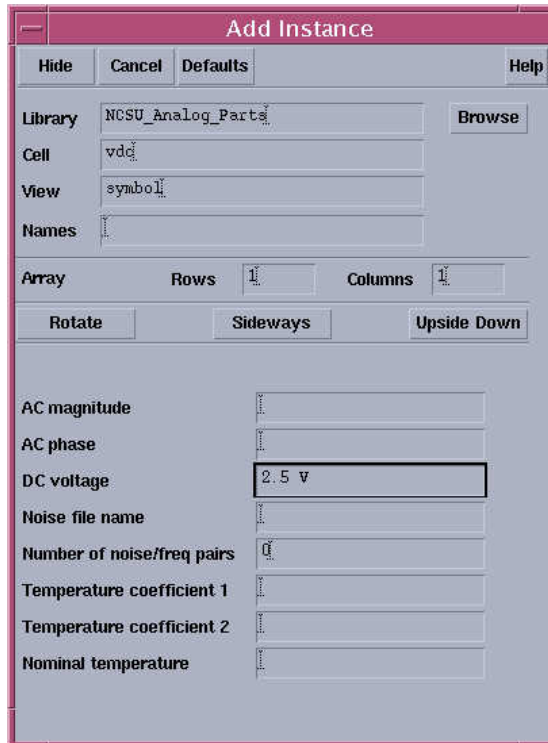
Figure 13. Adding the power supply (VDD from specification).

Add the load capacitor according to Figure 14. **Make sure it is 10f F not 10 F! This simulation will not work if the capacitance is too big!**

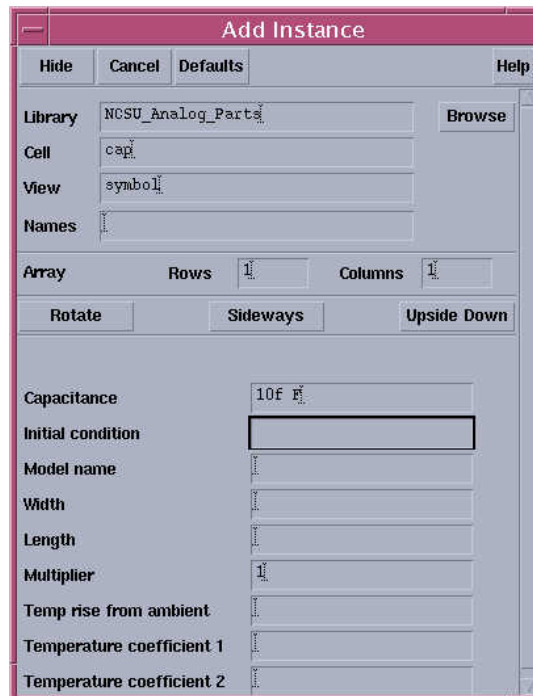Add the test vector (vpulse) according to Figure 15.

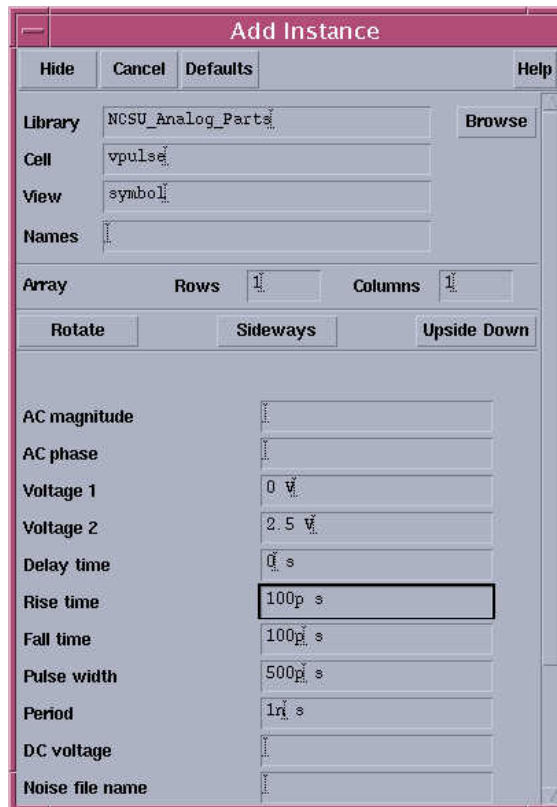Figure 14. Adding a load capacitor (10f F from specification).

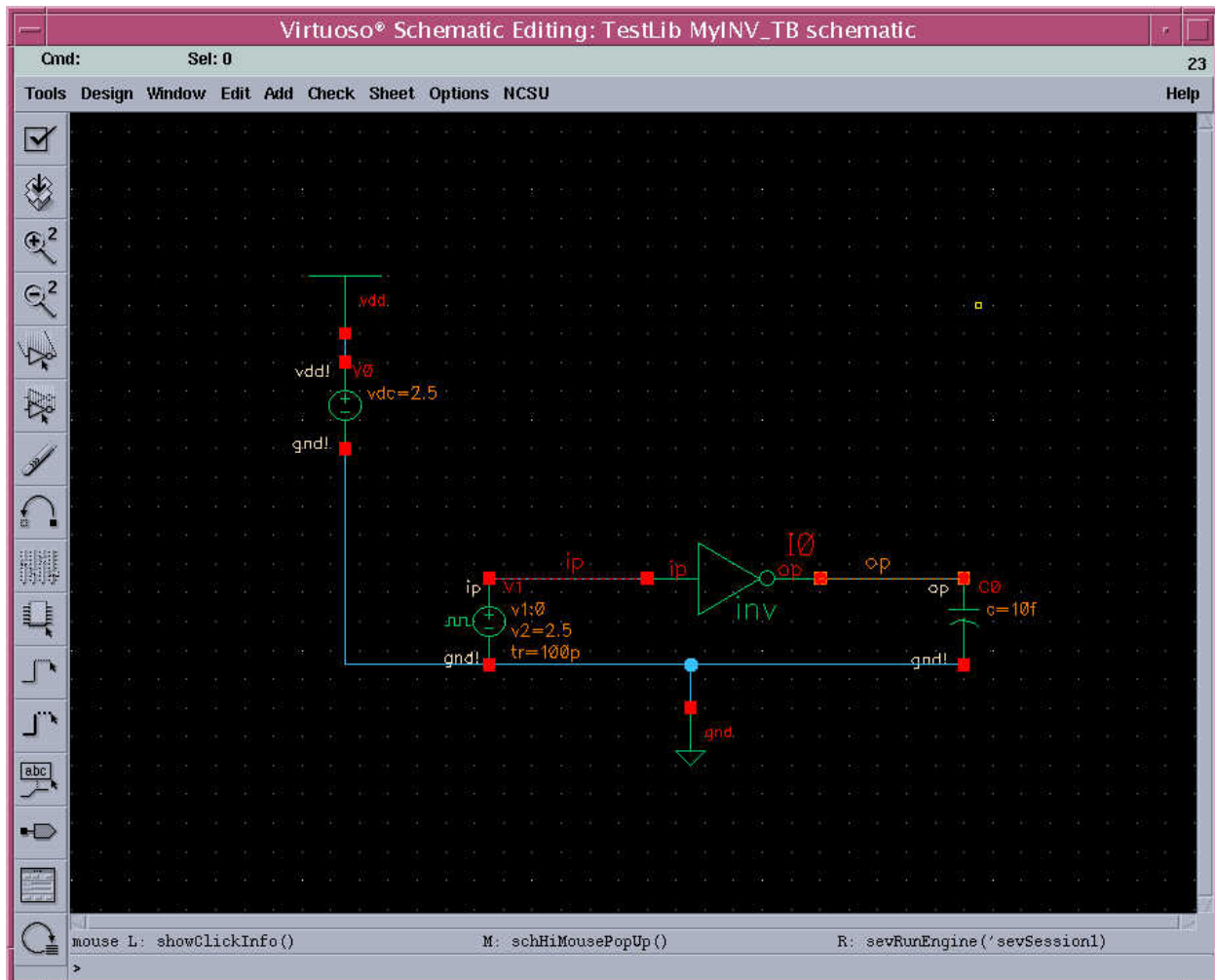Figure 15. Adding a test vector (From specification).

Figure 16. The completed test bench.

Press the esc key to get out of add instance mode. Move the symbols around as needed by pressing the 'm' key for move.

Press the esc key to get out of move mode and wire up the schematic according to Figure 16. Go to **Design->Check & Save** to check for errors. If you receive warnings and errors about pins being in one view and not the other, you have either name differences in the schematic vs. symbol or pin direction differences in schematic vs. symbol. The symbol should be perfect so check the schematic you did to make sure the pins are labeled correctly and the directions are correct.

You are now ready to simulate your inverter!

7. SIMULATION IN SPECTRE SPICE USING THE ANALOG DESIGN ENVIRONMENT

Now that you have created a schematic and symbolic view of your inverter and created a test bench in which to test your inverter, you are ready to run the Analog Design Environment tool. This is a tool to simulate your circuit in a physics-based environment that solves for voltages and currents over time. This is different from a functional simulation, which is just doing a high, low, Z or X analysis.

To simulate your circuit:

From the schematic editor window of your test bench circuit, go to **Tools->Analog environment**. A pop-up window like Figure 17 should appear. Since this is the first time you are running the Analog design tool, you will need to customize the environment.
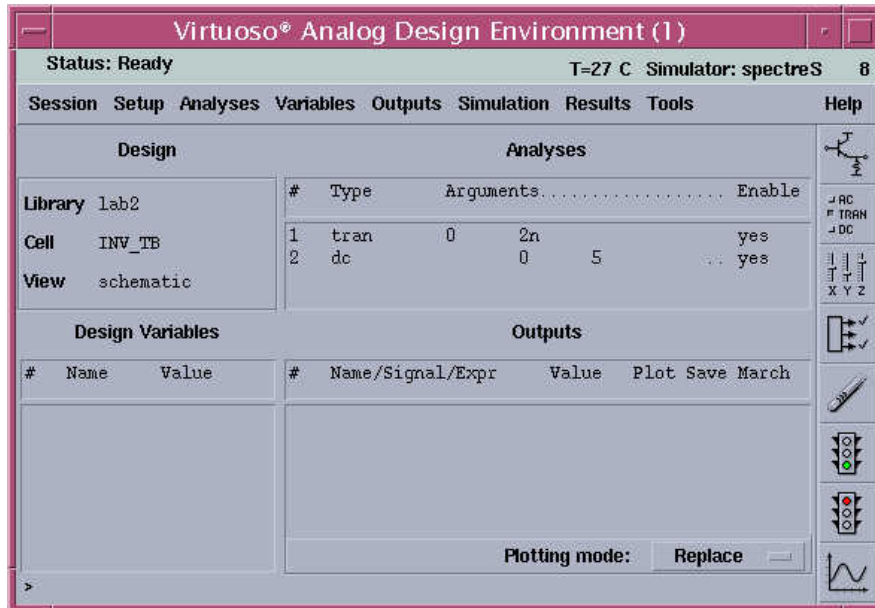

Figure 17. Analog Design Environment.

You will be using the Spectre Spice simulator, which is a spice-like simulator, using BSIM3 model decks, but the underlying algorithms are different. These algorithms are transparent to the user.

Go to **Setup->Simulator/Directory/Host**. A pop-up like Figure 18 should appear. Make sure the simulator is set to spectreS and click OK when done.
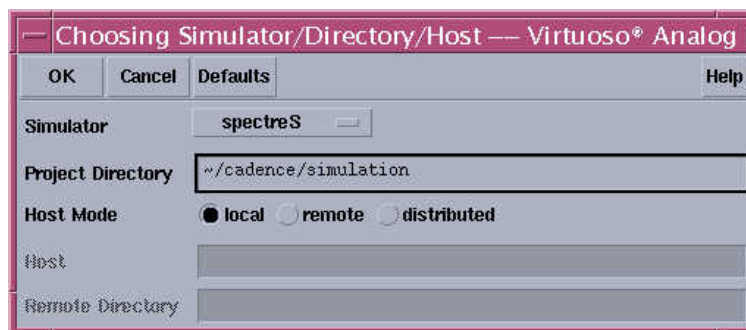

Figure 18. Setting up the simulator to use.

Now you need to make sure that Analog design tool can find the model decks for your process. Go to **Setup->Model path** and a pop-up like Figure 19 should appear. Add the model path as indicated in Figure 19.
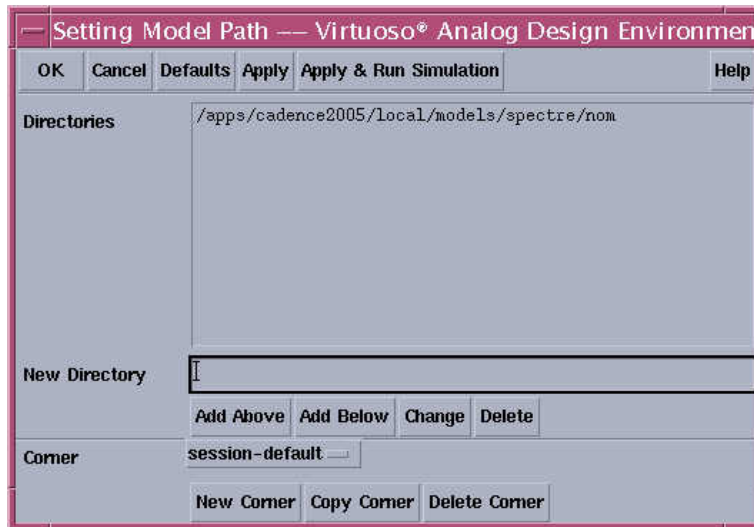
Figure 19. Setting up the model path.

Transient Analysis:

You will use the transient analysis to measure propagation delay times. To set up the transient analysis, go to **Analyses->Choose** and select the 'tran' radio button. Enter **2n** for the stop time of the transient analysis (equates to 2 nano-seconds).

DC Analysis:

In order to measure VINV (where VOUT=VIN), you need to do a DC analysis as well. VINV is a measure of the noise performance, and the closer VINV is to VDD/2, the better the noise performance of the inverter. Go to **Analyses->Choose** and fill out the pop-up according to Figure 20.

Click on Select Component and then in the schematic click on the vpulse.

Select VDC when the pop-up like Figure 21 appears.

Select the start and stop voltages to be 0 and 2.5. Your pop-up should look like Figure 22.
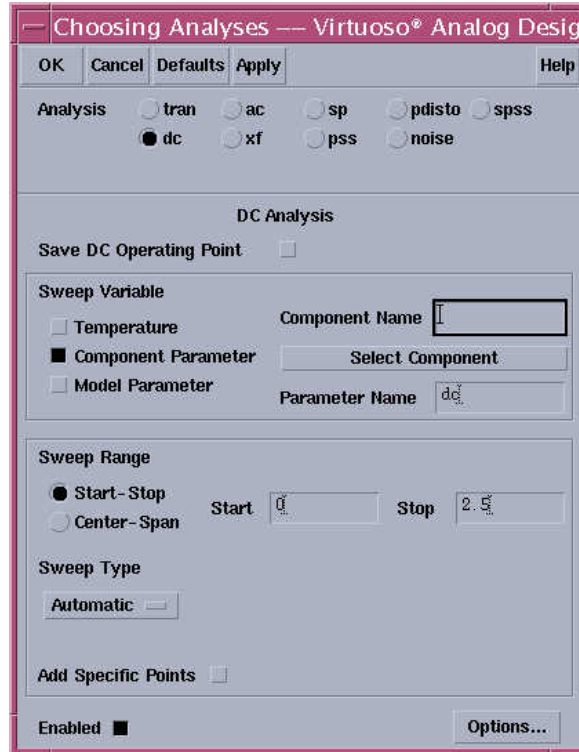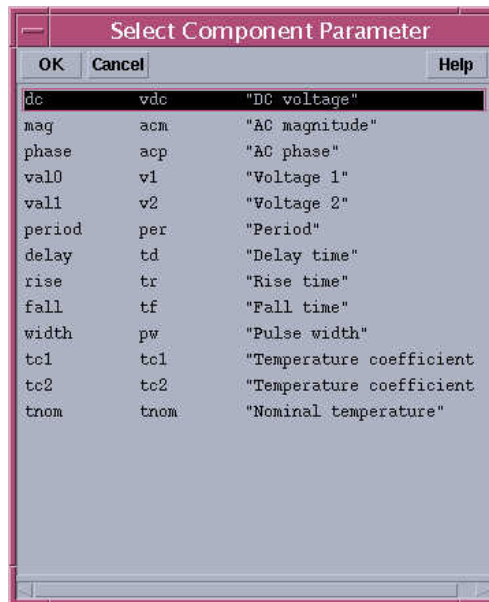
Figure 20. Setting up a DC analysis.

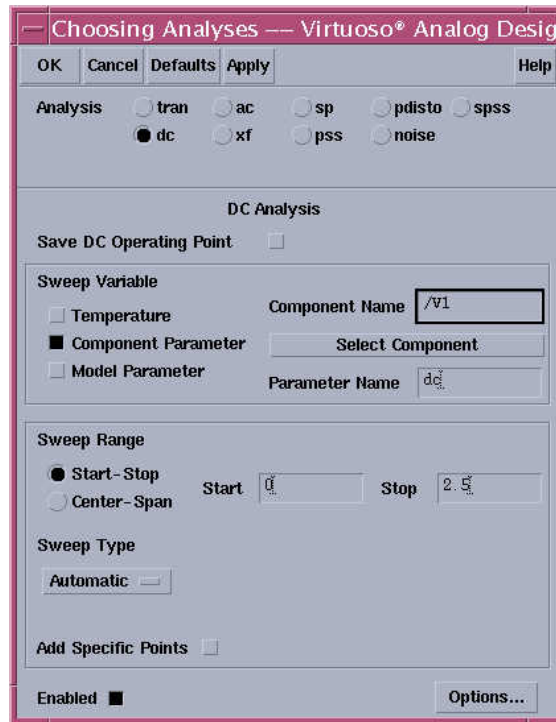Figure 21. Choosing to sweep DC voltage.

Figure 22. Completed DC Analysis Setup.

Adding Wire Names:

In order to easily see which signal is the input and which is the output, it is advisable to add wire names to the wires connecting A (input) and Y (output) of the inverter. Go to **Add->Wire names** and add names 'A' and 'Y' to the resulting window, as shown in Figure 23.
Select the inverter input net and then the inverter output net in your test bench schematic in order to 'name' the nets.
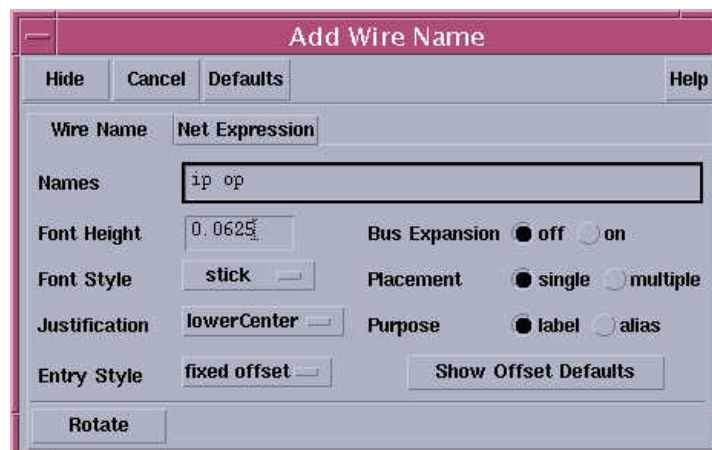

Figure 23. Adding Wire Names.

Choosing which nets to plot:

Now you need to choose which vectors you want to plot. Go to **Outputs->To be plotted->Select->on schematic**. Go back to your inverter test bench schematic and click on the net labeled 'ip' and the net labeled 'op'. Observe that the nets change color as you select them. (If you click directly on a pin it will probe the current, and the terminal of the device you clicked will have circles drawn around them. Clicking on a net, as you're doing here, probes the voltage.)

Press the esc key to get out of selection mode. Your Analog design window should now look like Figure 24.
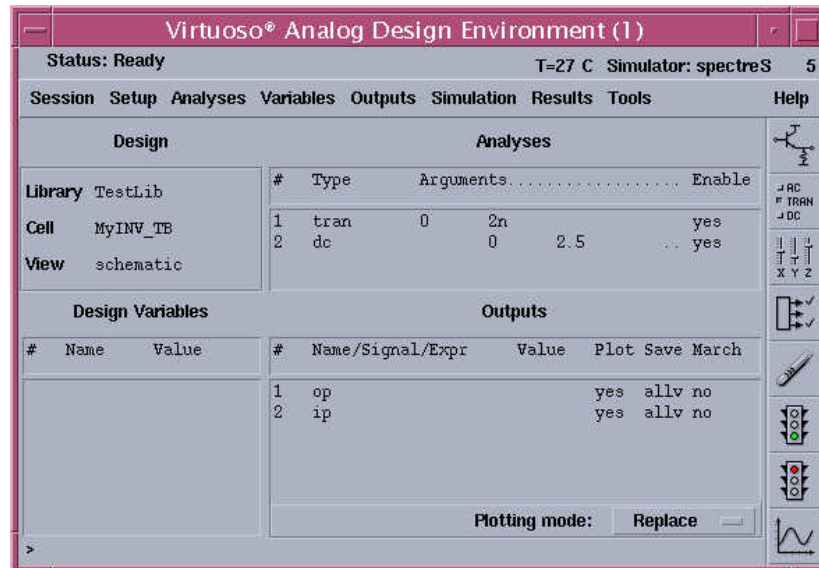

Figure 24. Selecting which vectors to plot.

In the Analog design tool, go to **Simulation->Run**. The CIW and the Analog design windows will show you the process it goes through to simulate your circuit. If all went well, a waveform window containing your transient and DC analyses should appear. Observe these waveforms to ensure that they match your expectations for your inverter circuit design.

If the simulations worked, go back to the CIW and go to **Options->Save defaults** and click OK on the pop-up window. This will save your simulator environment, but not your plot settings.

Note: The transient simulation should look similar to Figure 25. Go ahead and add markers (go to the Marker menu) on the input and output waveforms at the voltages shown in Figure 25 (you will use this for comparison purposes with the post-layout simulation).
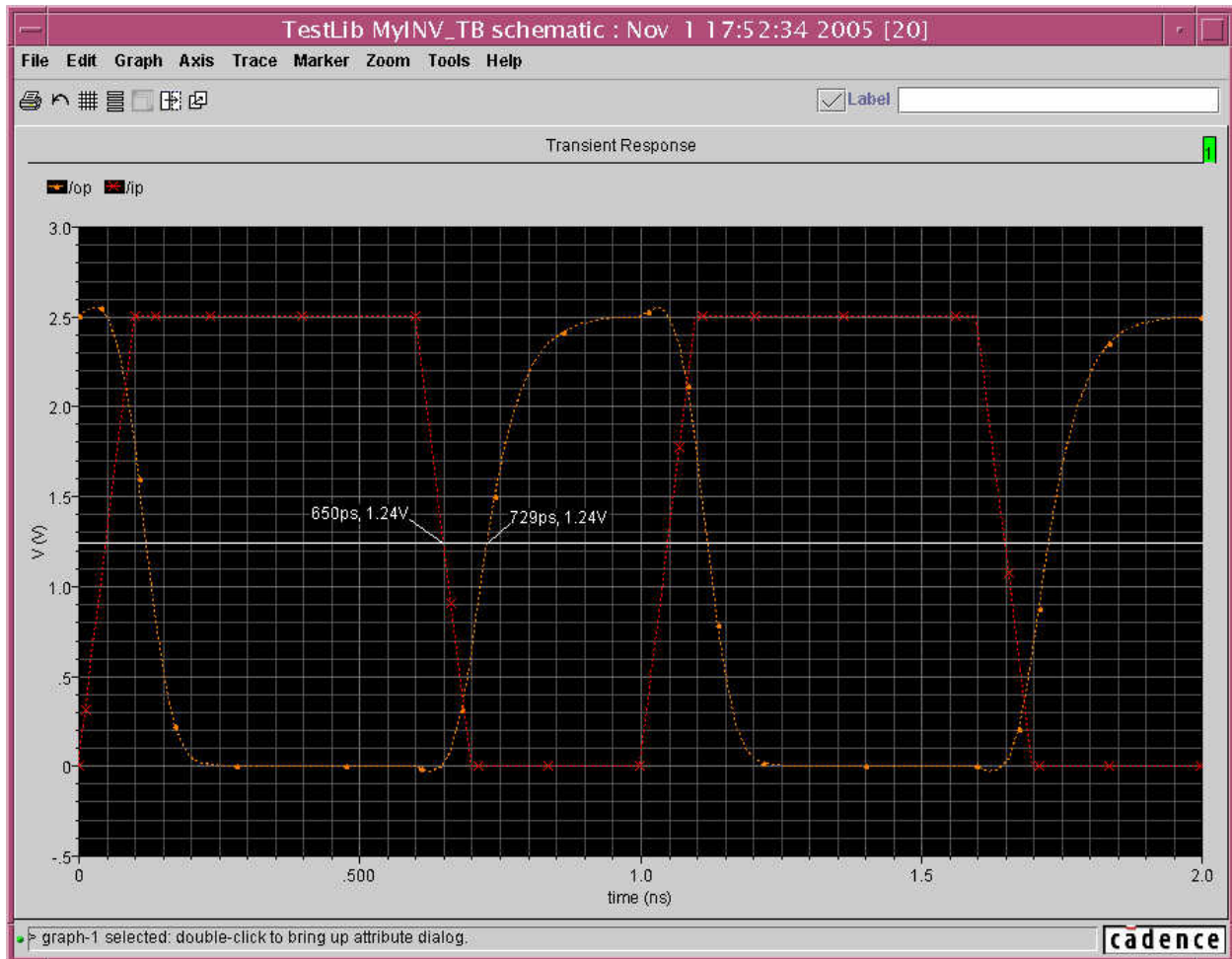
Figure 25. Transient Analysis.

Possible Simulation Problems:

Doh! The simulation did not work!

If you get error messages like "model XXX not found", you did not set the path correctly to point to the directory containing the models for your PMOS and NMOS FETs.

If you get a spice error message, you probably did not set your vpulse, or vdd correctly.

If it takes a long time to run, and/or the simulator times out, the capacitor could be too big, or the width or length of a MOSFET could have the wrong units (for example, instead of 4 microns it is 4 meters).

If the simulation runs but the output does not look correct, the capacitor could be too big or the DC voltage may not be set correctly.

To fix or change properties of the inverter circuit, go to **Design->Hierarchy->descend edit** and click on your inverter. Change the pop-up to schematic and click OK. To edit a MOSFET or anything else on your inverter circuit, press 'q' and click on what you want to edit. To return to the top level (the level of your test bench), go to **Design->Hierarchy->Return to the top**.

Saving your State:

In order to save certain setup specifications in your simulation, save the state. To do this, go to **Session->Save the state** in your Analog design window.

8. POST LAYOUT SIMULATION

Now, you will extract the parasitic capacitances from your inverter layout (done in Tutorial 1) in order to include them with your transient simulation.
First, open up your inverter layout from the Library Manager window. Go to **Verify->Extract**.
Click on **Set Switches** and select **Extract_parasitic_caps** in the resulting window and click OK. Your Extractor window should now look similar to Figure 26.
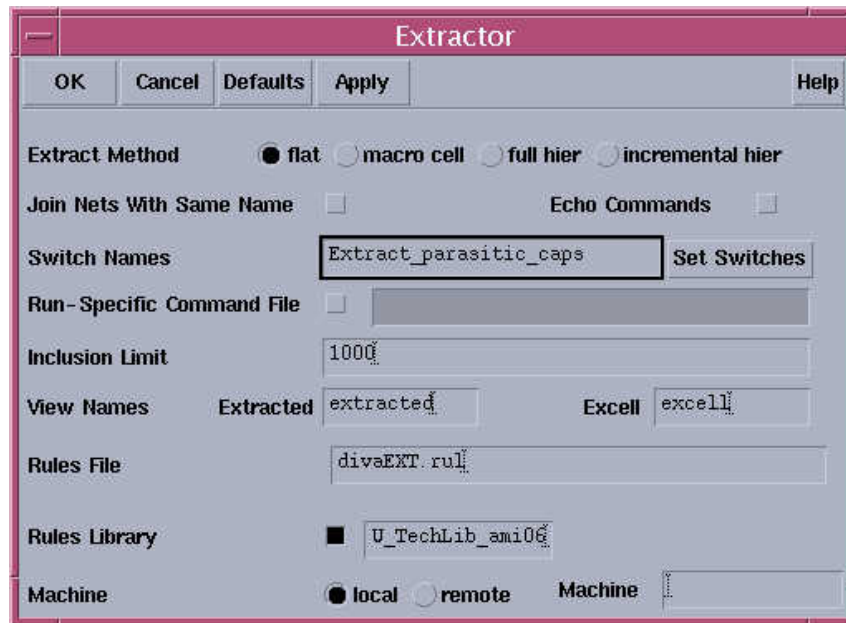

Figure 26. Extractor Window.

Click on OK to perform this operation. Now close the layout view of your design. Bring up the extracted view of your layout by double-clicking it from the library manager. Next, you will perform a layout-versus-schematic comparison as a design check. Go to **Verify->LVS** and you will see the window as shown in Figure 27. Fill it out according to this window.
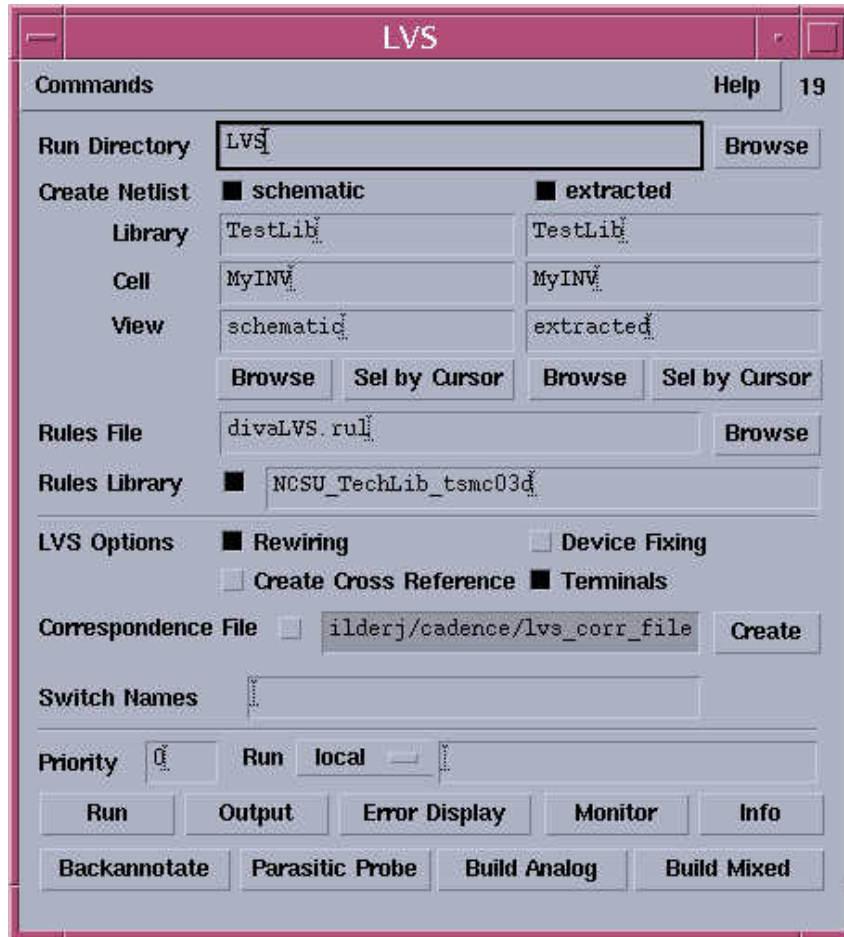
Figure 27. LVS Window.

Click **Run** and wait *patiently* for a popup window to tell you that the LVS process has completed successfully. Note that this it not telling you that the layout and schematic netlists are identical. To find out the results from the LVS, click on **Output**. Determine if the netlists match from the resulting window.

After ensuring that the netlists match, in the LVS window, select "Build Analog". This creates a file called analog_extracted (in the same cell view that contains your layout and schematic). You will use this file when doing the transient analysis in the Analog Design Environment.

Go back to the Analog Design Environment window, and go to **Setup->Environment**, and insert "analog_extracted" in front of "schematic" in the Switch View List, as shown in Figure 28.
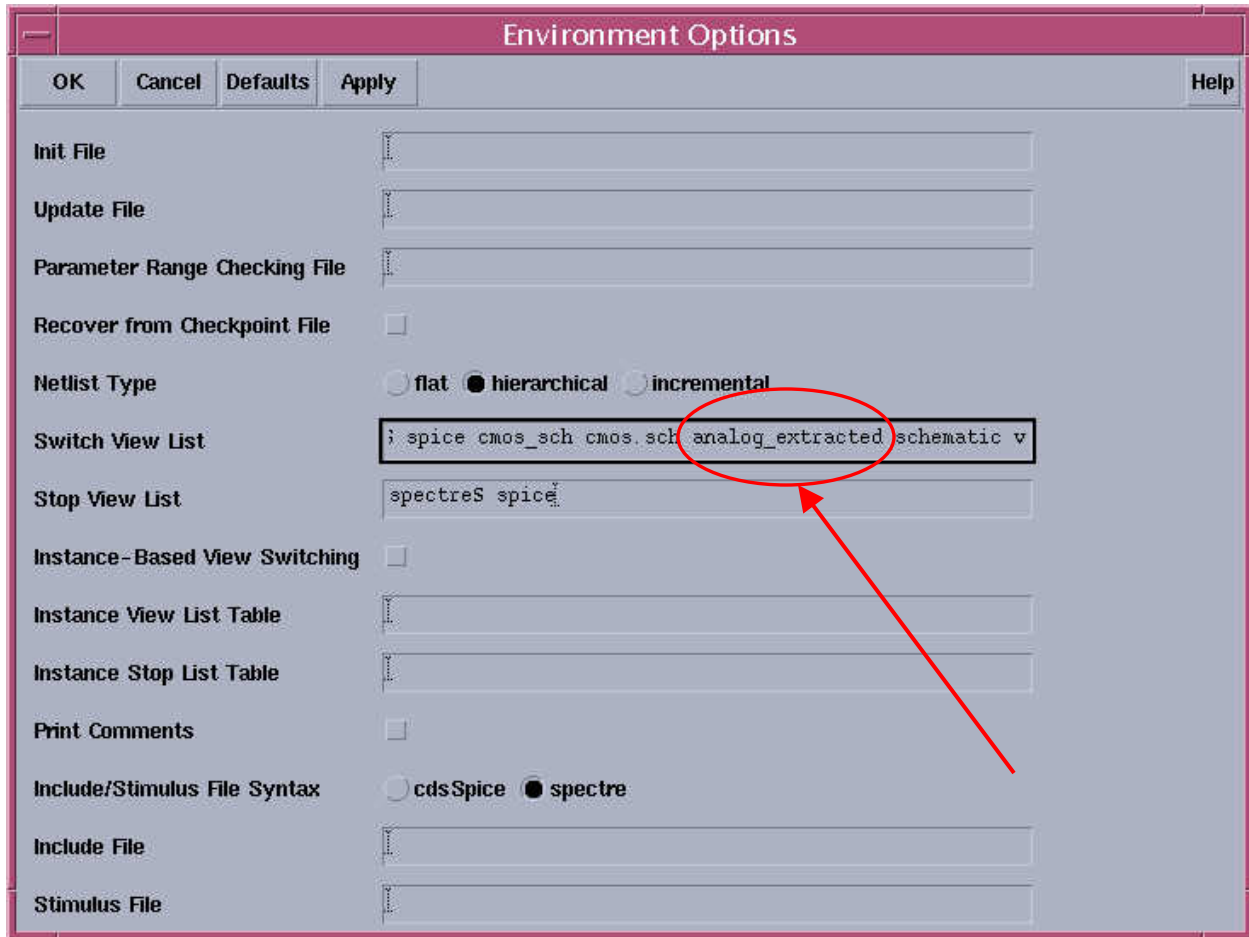
Figure 28. Environment Options.

Run the transient analysis, and your waveform should look similar to Figure 29. (Place markers at the voltages shown, and verify that the timing is different from your previous results.)
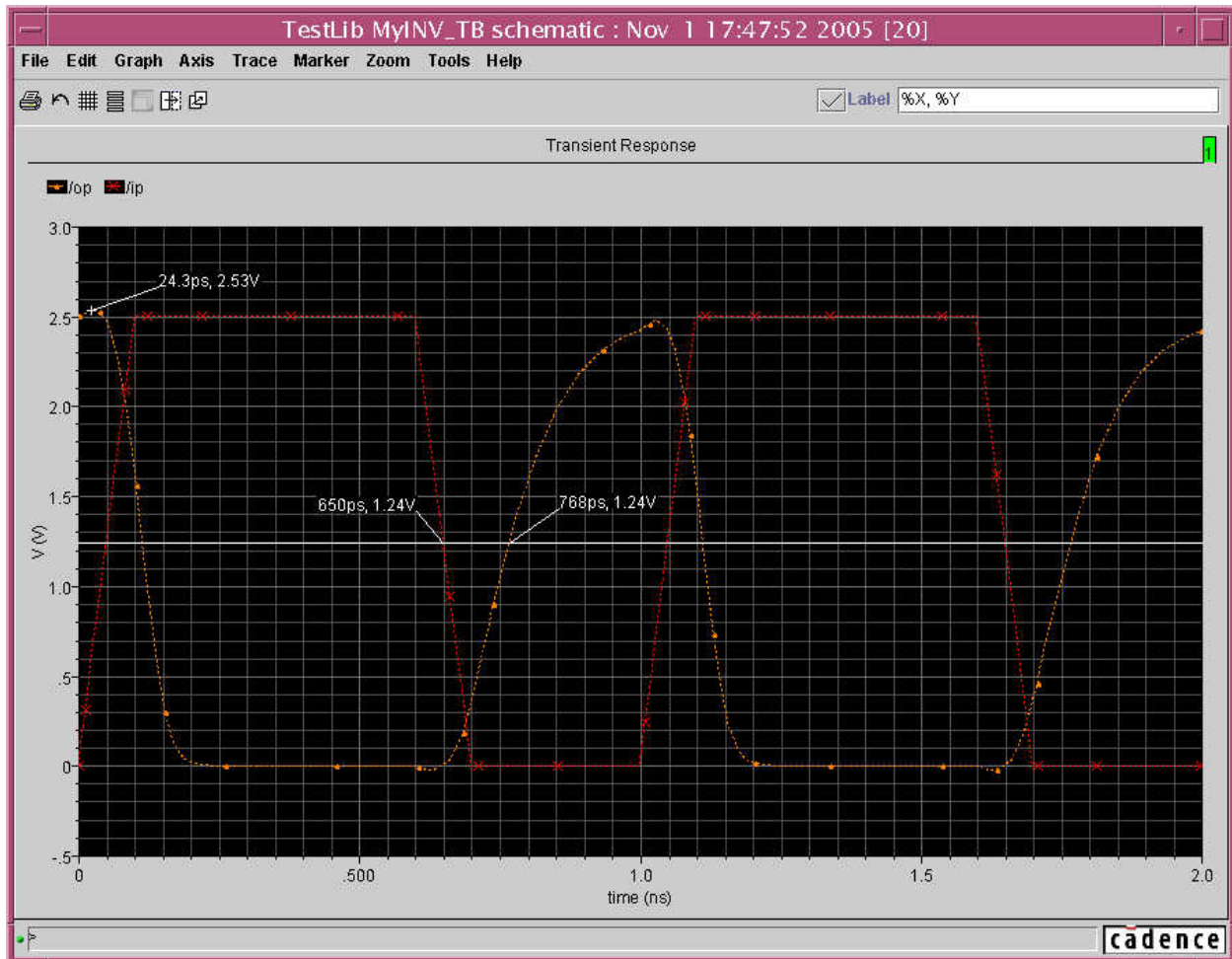
Figure 29. Transient Analysis with Parasitic Capacitances.

9. TWO-INPUT NAND GATE ANALYSIS

Using the procedure developed and demonstrated in the inverter circuit design/test, design a two-input NAND gate circuit (shown in Figure 26 for your reference) with accompanying symbol, and then create a test bench schematic for simulation purposes (you will not do a layout here!).
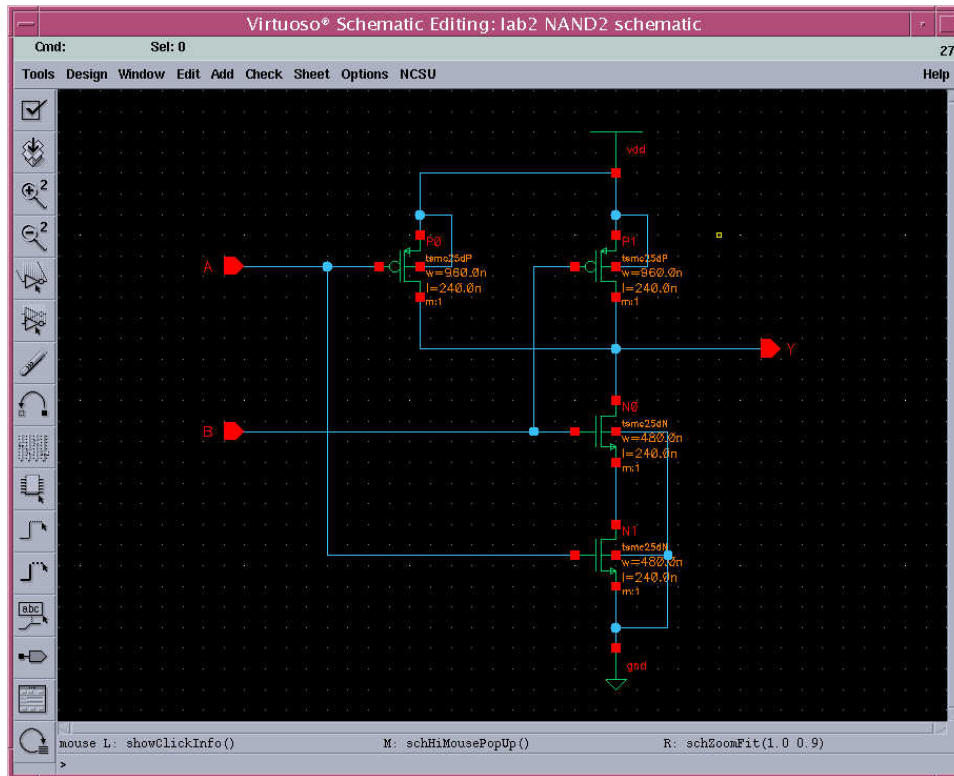
Figure 26. Two-input NAND Gate Circuit.

10. ASSIGNMENT

- Turn in the transient analysis waveform printouts from your inverter:
  - Without parasitic capacitances (20%)
  - With parasitic capacitances (20%)
- To demonstrate your design and test procedure, hand in the following printouts:
  - your two-input NAND gate circuit (10%)
  - your two-input NAND gate test bench circuit (10%)
- To prove the operation of your NAND gate circuit, hand in printouts of the transient analysis waveforms of the inputs and output to prove the entire truth table shown in Table 1 (40%)

Input 1	Input 2	Output	Grade %
0	0	1	10
0	1	1	10
1	0	1	10
1	1	0	10

Table 1. Two-Input NAND Gate Truth Table.