CPE/EE 427, CPE 527
VLSI Design I
CMOS Inverter

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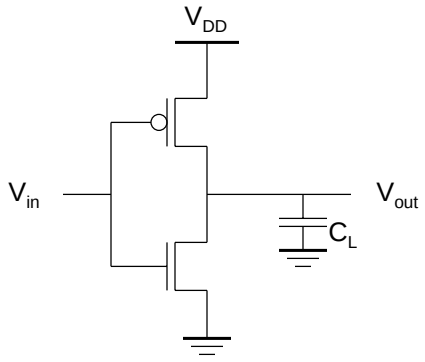
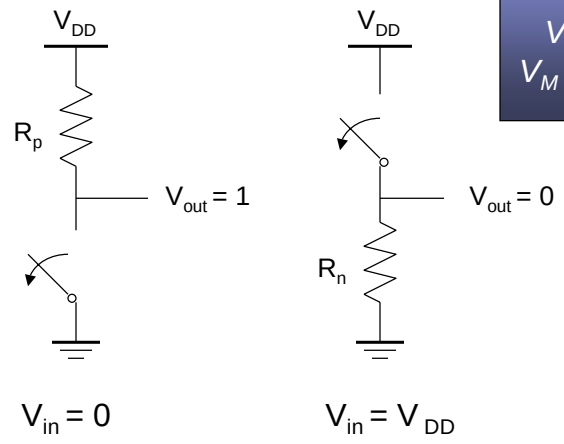
CMOS Inverter:
A First Look



CMOS Inverter:
Steady State Response

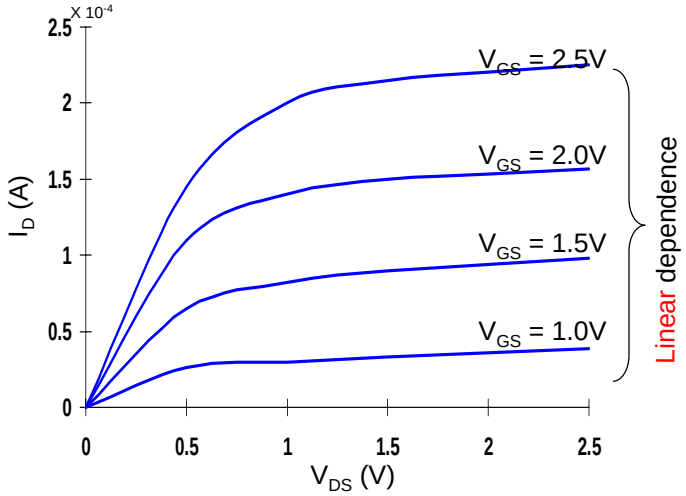


$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

CMOS Properties

- Full rail-to-rail swing ⇒ high noise margins
  - Logic levels not dependent upon the relative device sizes ⇒ transistors can be minimum size ⇒ ratioless
- Always a path to V_{dd} or GND in steady state ⇒ low output impedance (output resistance in kΩ range) ⇒ large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) ⇒ nearly zero steady-state input current
- No direct path steady-state between power and ground ⇒ no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors

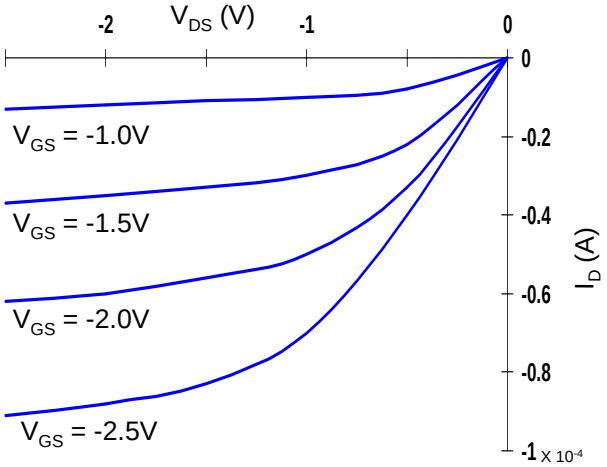
Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

Short Channel I-V Plot (PMOS)

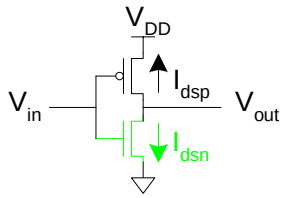
- All polarities of all voltages and currents are reversed



PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

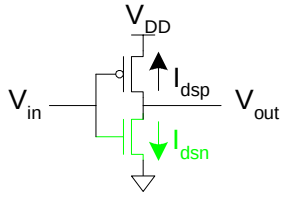
nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} <$	$V_{gsn} >$ $V_{dsn} <$	$V_{gsn} >$ $V_{dsn} >$



nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

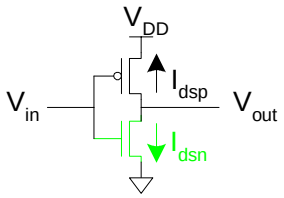


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$

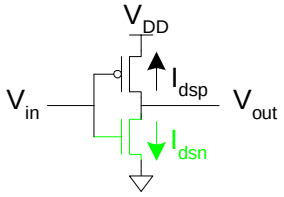


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

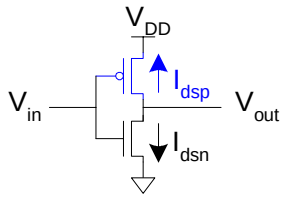
$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$



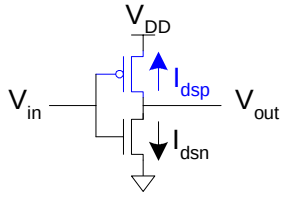
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} >$	$V_{gsp} <$ $V_{dsp} >$	$V_{gsp} <$ $V_{dsp} <$



pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$



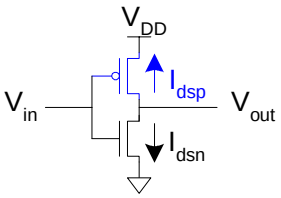
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$



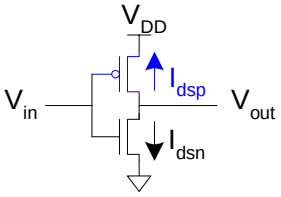
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

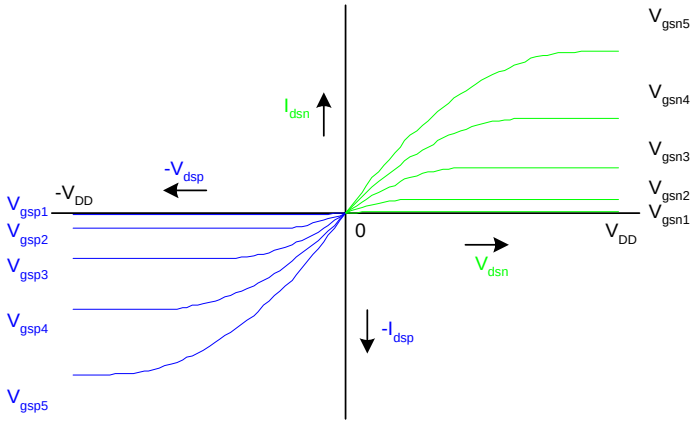
$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$

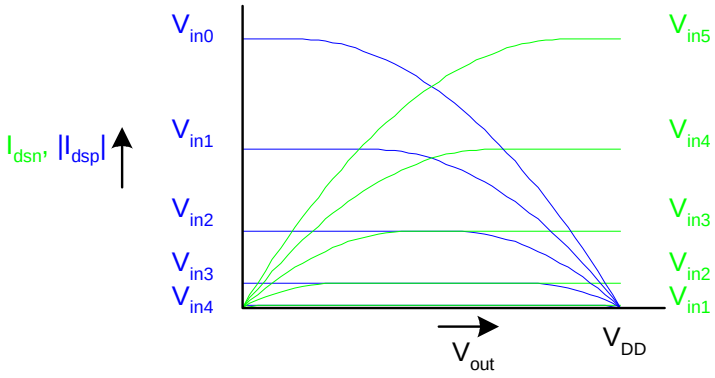


I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

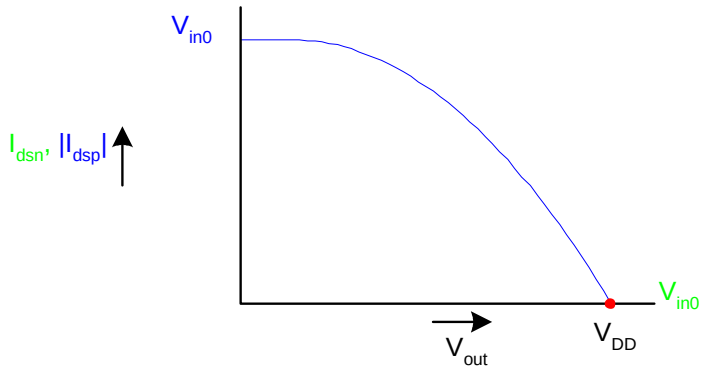


Current vs. V_{out}, V_{in}



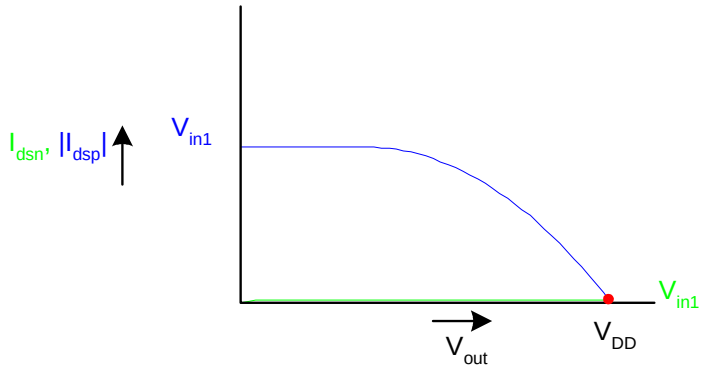
Load Line Analysis

- $V_{in} = 0$



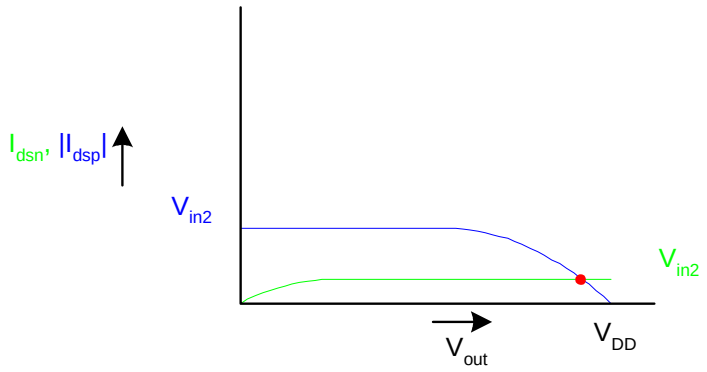
Load Line Analysis

- $V_{in} = 0.2V_{DD}$



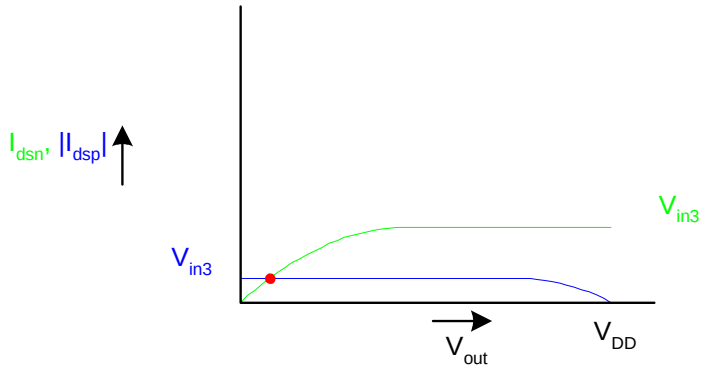
Load Line Analysis

- $V_{in} = 0.4V_{DD}$



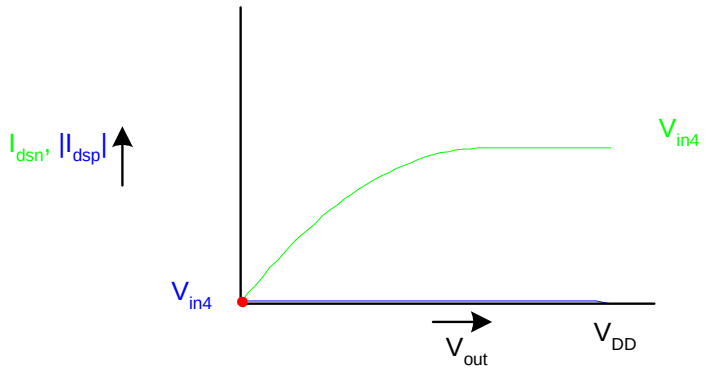
Load Line Analysis

- $V_{in} = 0.6V_{DD}$



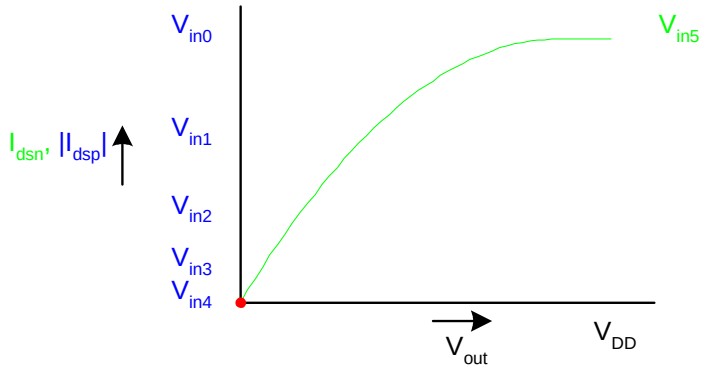
Load Line Analysis

- $V_{in} = 0.8V_{DD}$

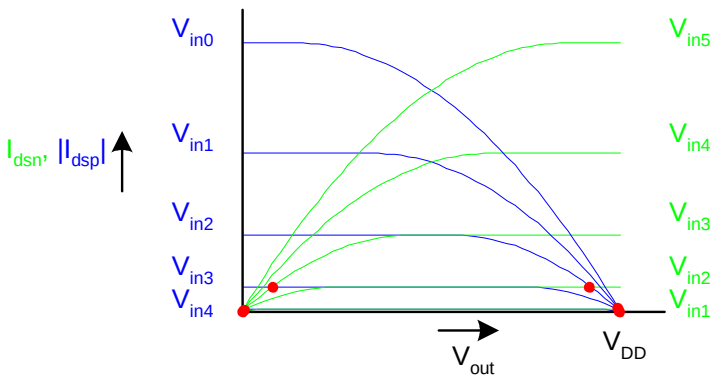


Load Line Analysis

- $V_{in} = V_{DD}$

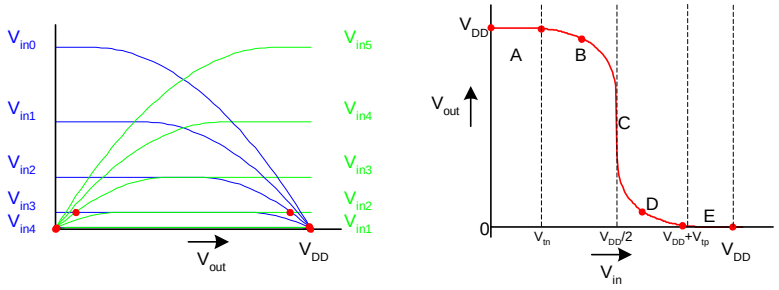


Load Line Summary

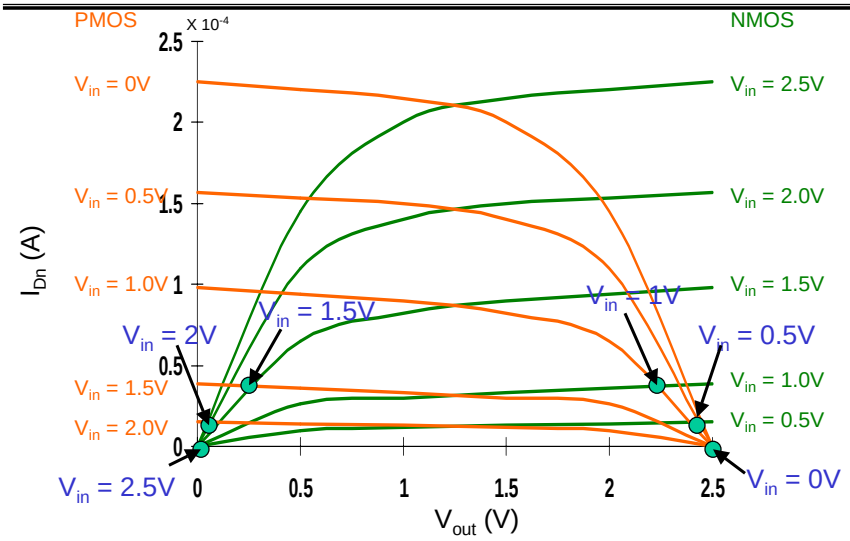


DC Transfer Curve

- Transcribe points onto V_{in} vs. V_{out} plot

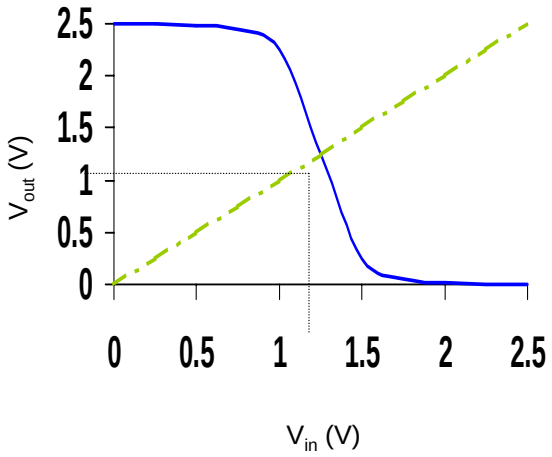


CMOS Inverter Load Lines



0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$

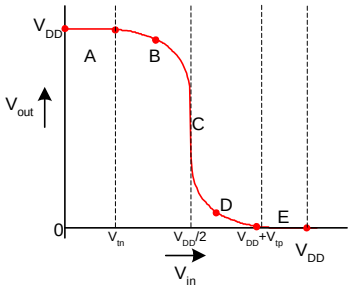
CMOS Inverter VTC



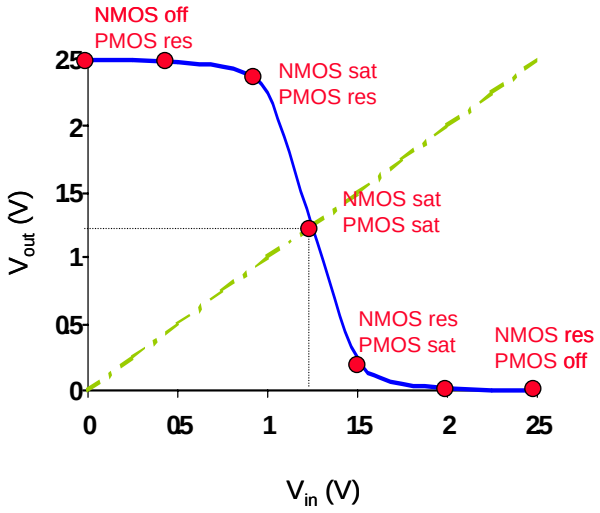
Operating Regions

- Revisit transistor operating regions

Region	nMOS	pMOS
A		
B		
C		
D		
E		

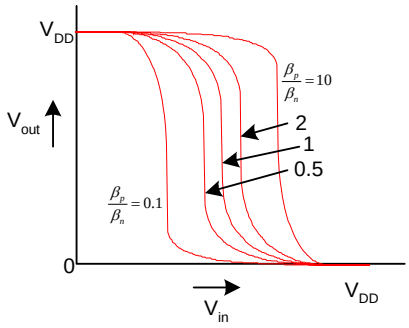


CMOS Inverter VTC



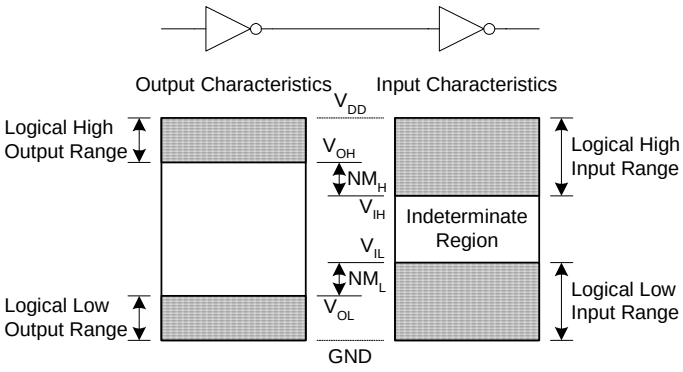
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



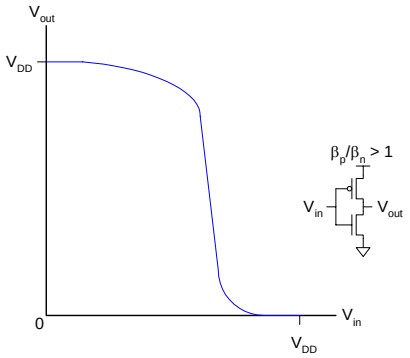
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



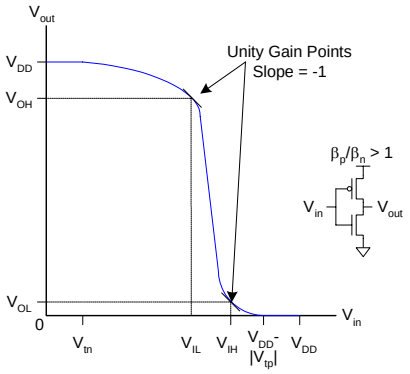
Logic Levels

- To maximize noise margins, select logic levels at

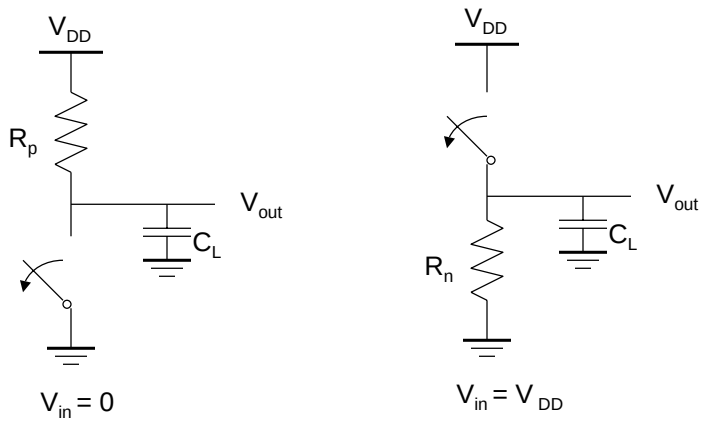


Logic Levels

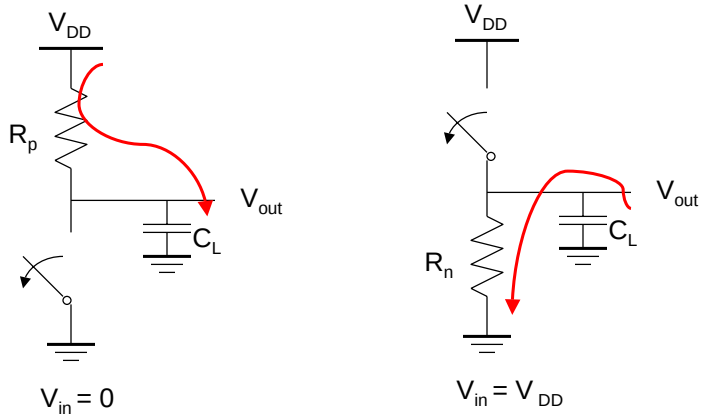
- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



CMOS Inverter:
Switch Model of Dynamic Behavior



CMOS Inverter:
Switch Model of Dynamic Behavior



Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

Switching Threshold

- V_M where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)

  $$V_M \approx rV_{DD}/(1 + r) \text{ where } r = k_pV_{DSATp}/k_nV_{DSATn}$$

- Switching threshold set by the ratio r, which compares the relative driving strengths of the PMOS and NMOS transistors

- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n'V_{DSATn}(V_M-V_{Tn}-V_{DSATn}/2)}{k_p'V_{DSATp}(V_{DD}-V_M+V_{Tp}+V_{DSATp}/2)}$$

Switch Threshold Example

- In our generic 0.25 micron CMOS process, using the process parameters from slide L03.25, a V_{DD} = 2.5V, and a minimum size NMOS device ($(W/L)_n$ of 1.5)

	V_{T0}(V)	$\gamma(V^{0.5})$	V_{DSAT}(V)	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} =$$

Switch Threshold Example

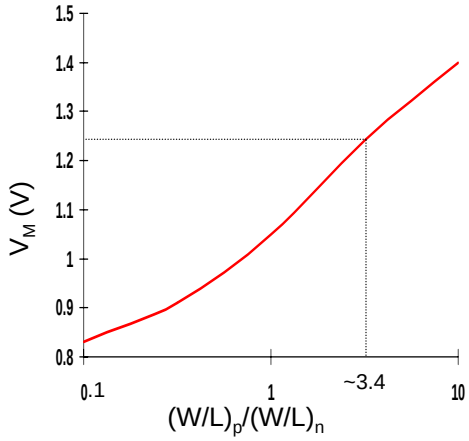
- In our generic 0.25 micron CMOS process, using the process parameters, a V_{DD} = 2.5V, and a minimum size NMOS device ($(W/L)_n$ of 1.5)

	V_{T0}(V)	$\gamma(V^{0.5})$	V_{DSAT}(V)	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

$$(W/L)_p = 3.5 \times 1.5 = 5.25 \text{ for a } V_M \text{ of } 1.25V$$

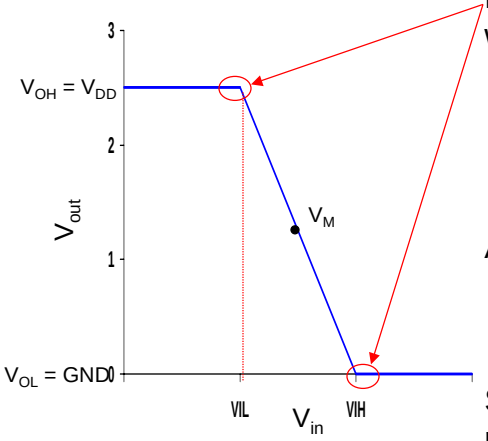
Simulated Inverter V_M



Note: x-axis is semilog

- V_M is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives V_M's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves V_M towards V_{DD}
- Increasing the width of the NMOS moves V_M toward GND

Noise Margins Determining V_{IH} and V_{IL}



A piece-wise linear approximation of VTC

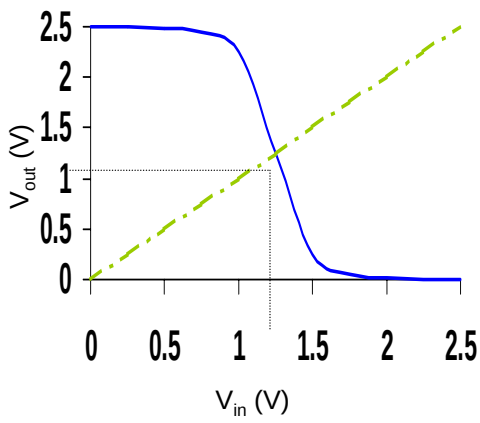
By definition, V_{IH} and V_{IL} are where $dV_{out}/dV_{in} = -1$ (= gain)

$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL} - GND$

Approximating:
$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

So high gain in the transition region is very desirable

CMOS Inverter VTC from Simulation



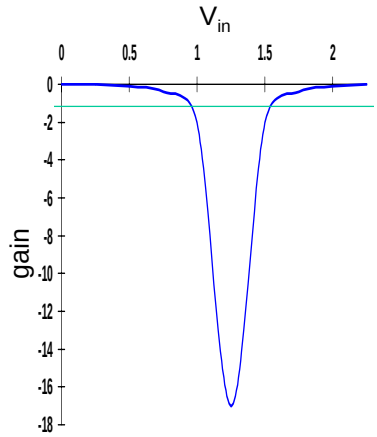
0.25um, $(W/L)_p/(W/L)_n = 3.4$
$(W/L)_n = 1.5$ (min size)
$V_{DD} = 2.5V$

$V_M \approx 1.25V$, $g = -27.5$

$V_{IL} = 1.2V$, $V_{IH} = 1.3V$
$NM_L = NM_H = 1.2$
(actual values are
$V_{IL} = 1.03V$, $V_{IH} = 1.45V$
$NM_L = 1.03V$ & $NM_H = 1.05V$)

Output resistance
low-output = 2.4kΩ
high-output = 3.3kΩ

Gain Determinates

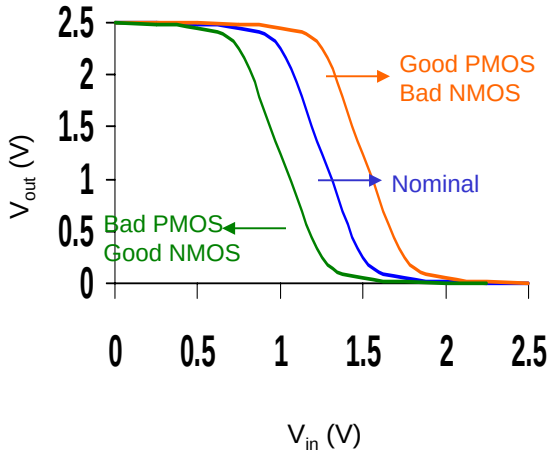


Gain is a strong function of the slopes of the currents in the saturation region, for $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

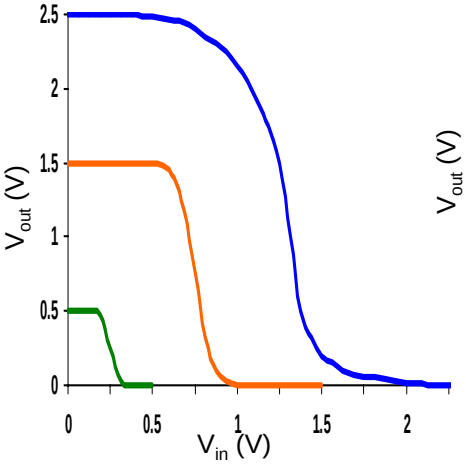
Determined by technology parameters, especially channel length modulation (λ). Only designer influence through supply voltage and V_M (transistor sizing).

Impact of Process Variation on VTC Curve

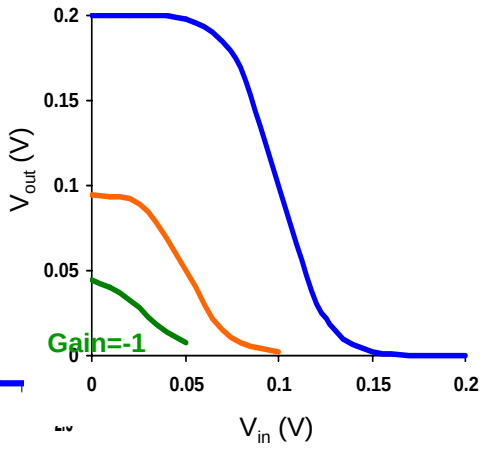


process variations (mostly) cause a shift in the switching threshold

Scaling the Supply Voltage



Device threshold voltages are kept (virtually) constant



Device threshold voltages are kept (virtually) constant