CPE/EE 427, CPE 527
VLSI Design I
Delay Estimation

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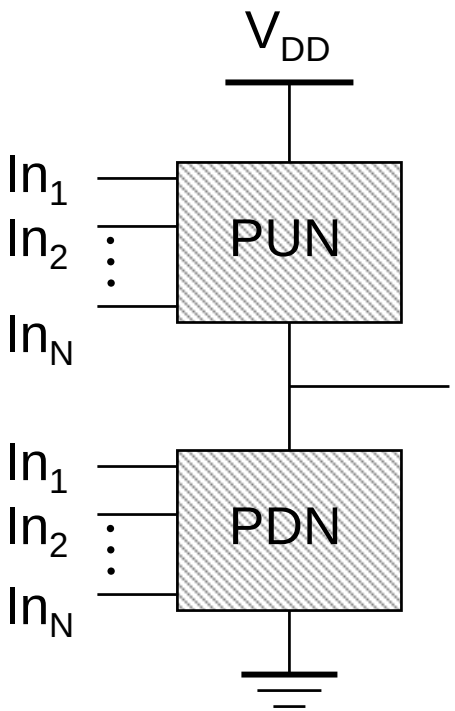
Review: CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - VOH and VOL are at VDD and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between VDD and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)
- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

Review: Static Complementary CMOS

Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

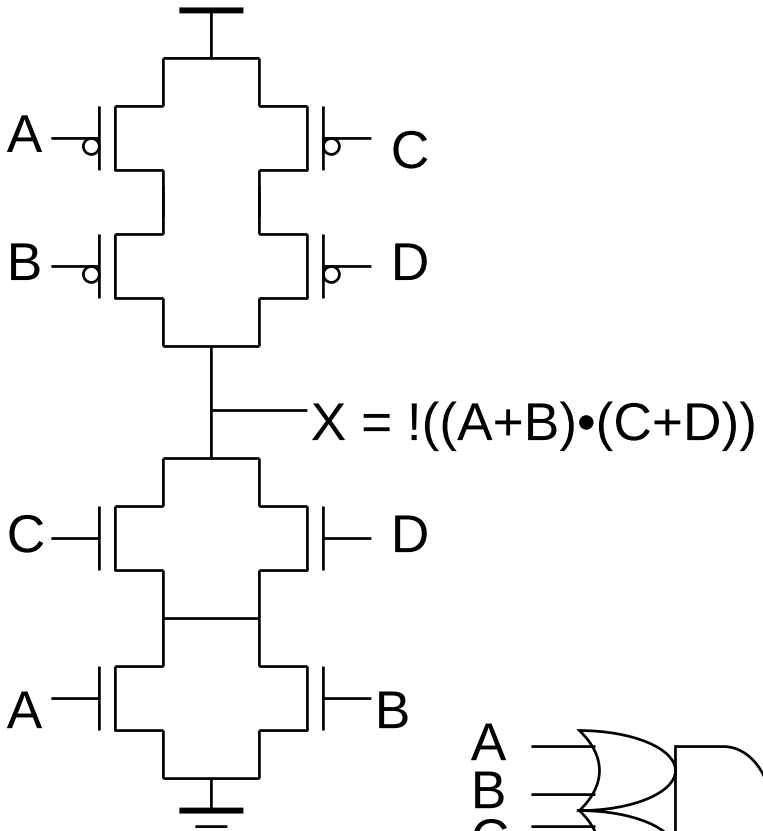
pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

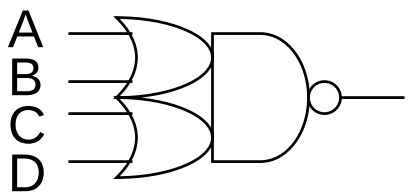
pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

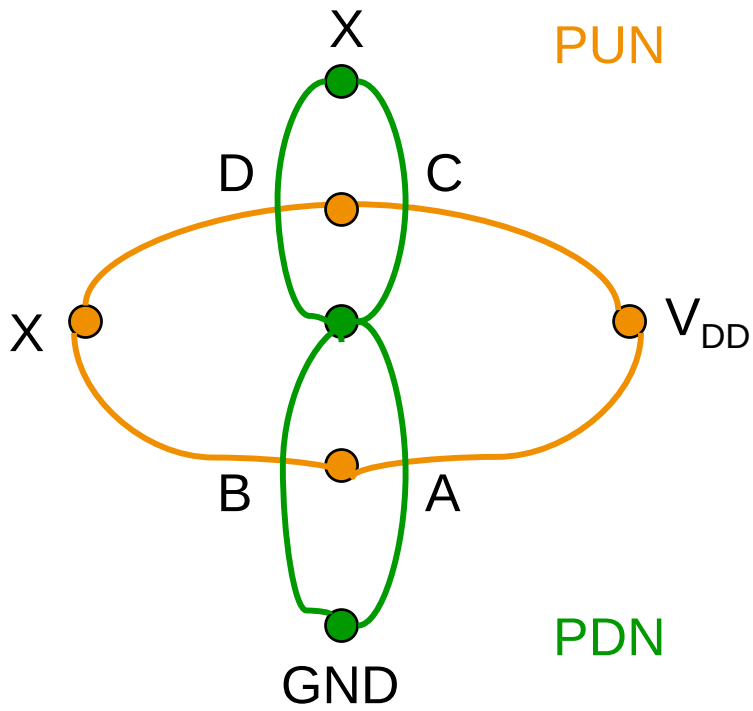
NMOS transistors only

PUN and PDN are dual logic networks

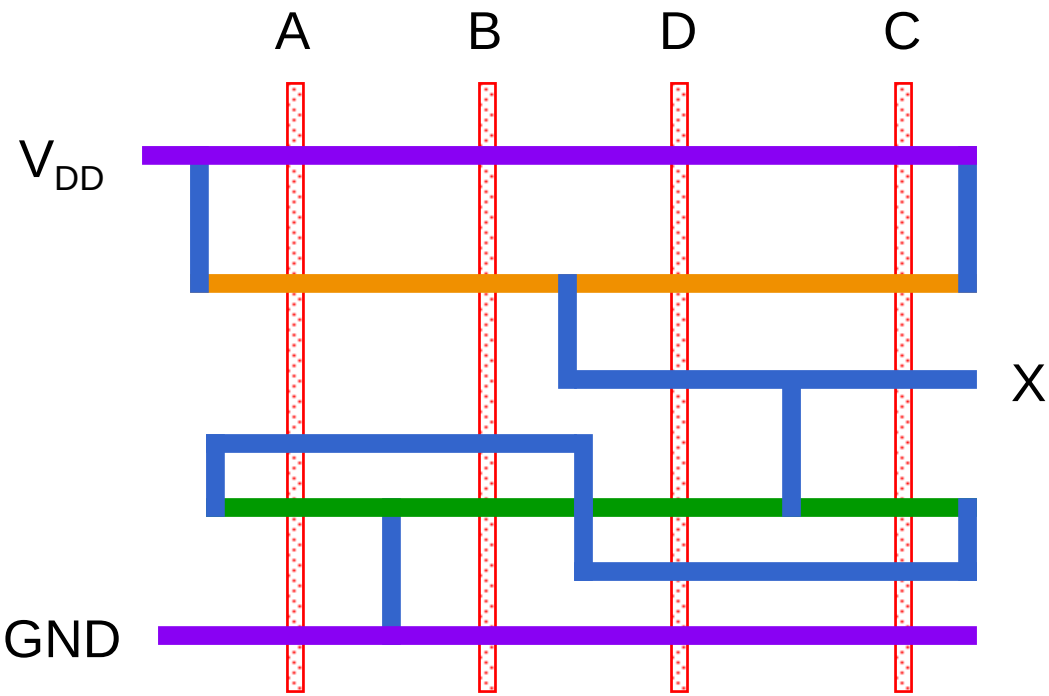
Review: OAI22 Logic Graph





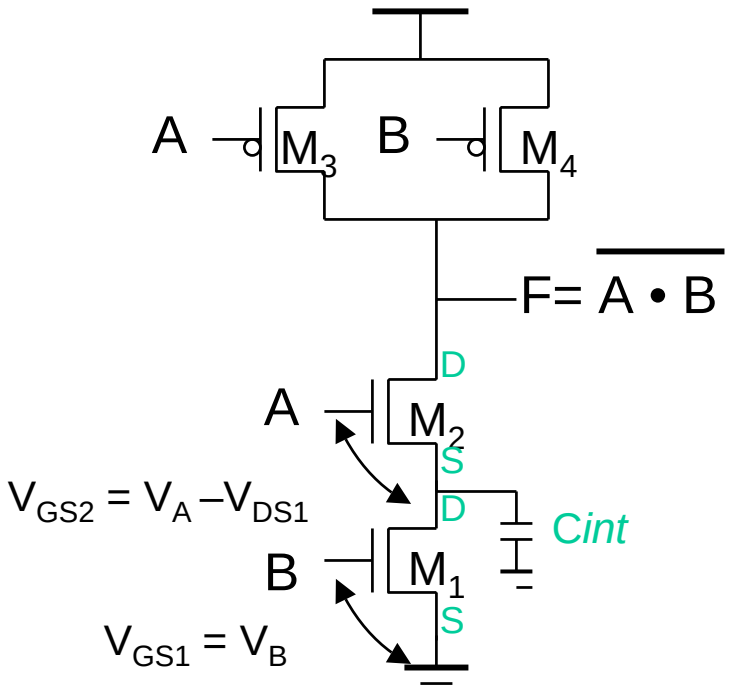


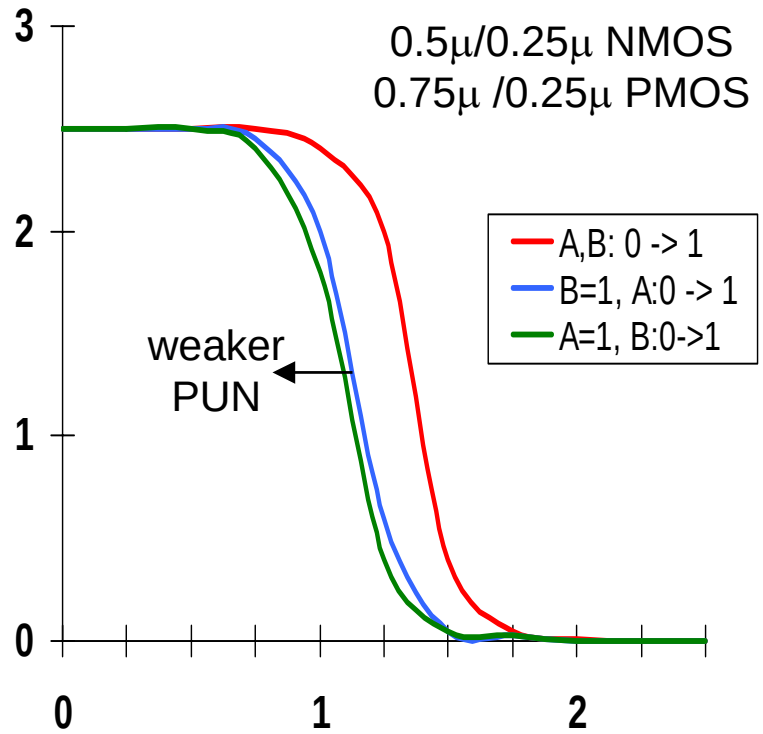
Review: OAI22 Layout



- Some functions have no consistent Euler path like x = !(a + bc + de) (but x = !(bc + a + de) does!)

Review: VTC is Data-Dependent





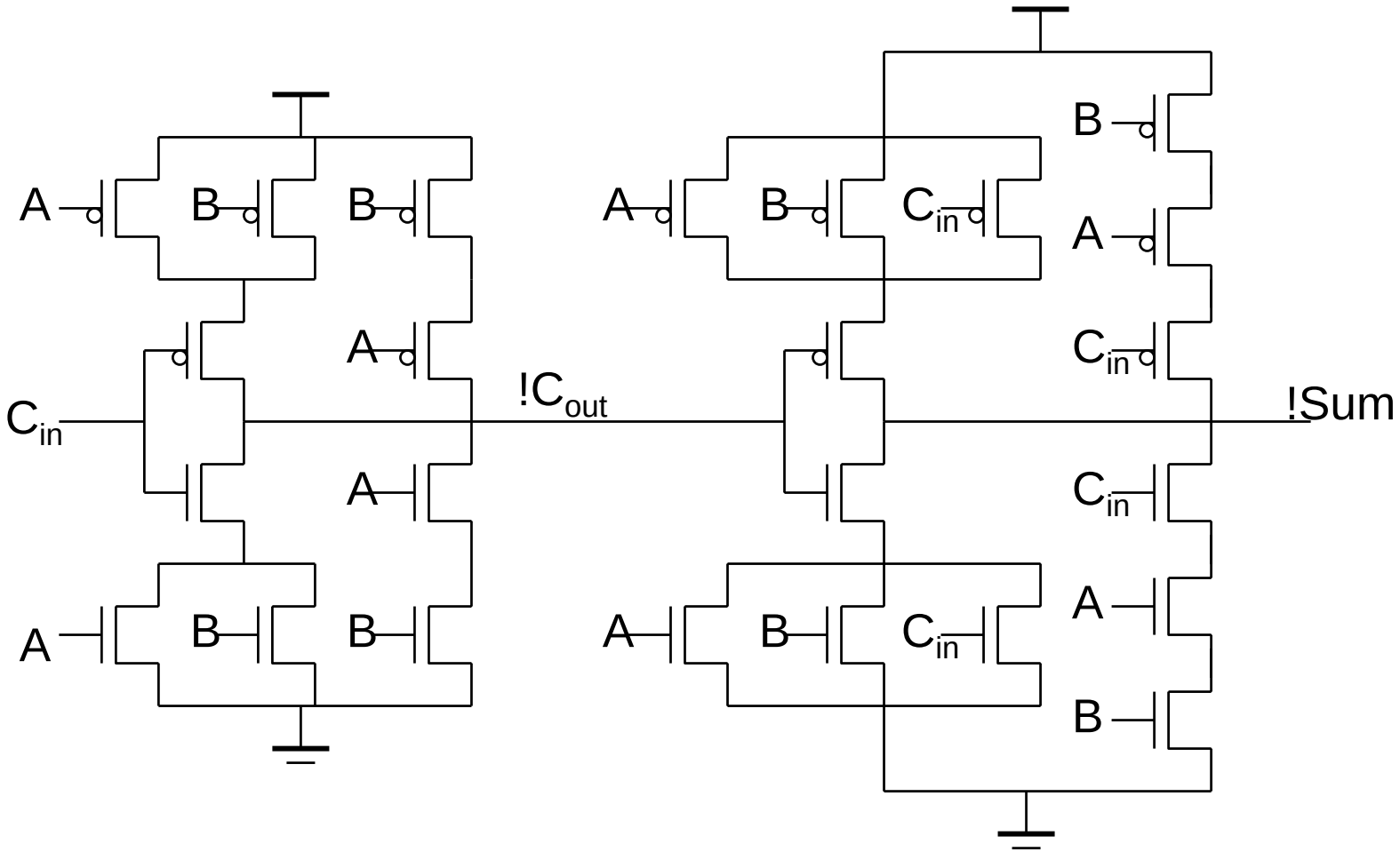
- The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

$V_{Tn1} = V_{Tn0}$

$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{(|2\phi_F| + V_{int}) - \sqrt{|2\phi_F|})}$

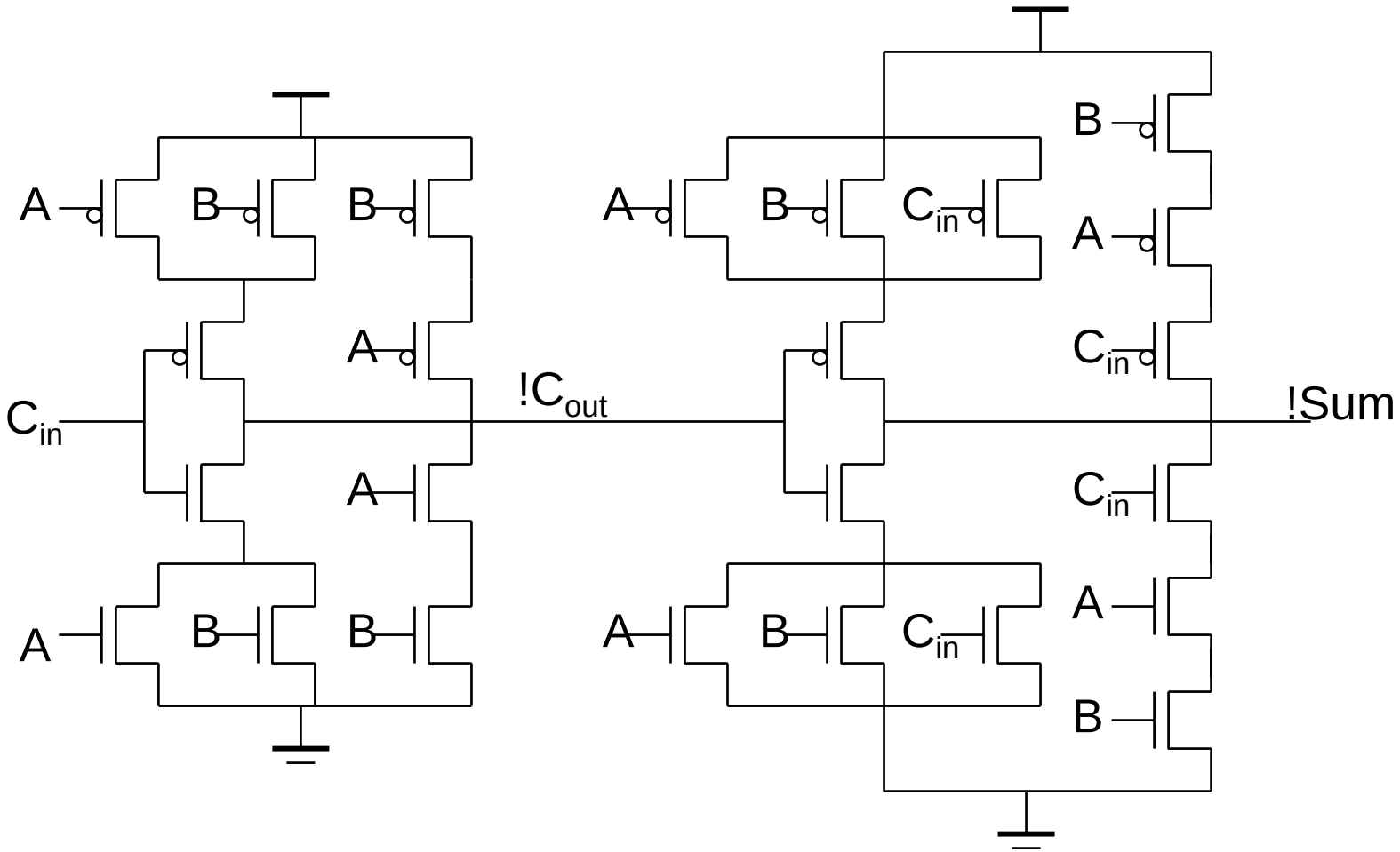
since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of C*int*

Static CMOS Full Adder Circuit



Static CMOS Full Adder Circuit

$!C_{out} = !C_{in} \,\&\, (!A \mid !B) \mid (!A \,\&\, !B)$ $!Sum = C_{out} \,\&\, (!A \mid !B \mid !C_{in}) \mid (!A \,\&\, !B \,\&\, !C_{in})$



$C_{out} = C_{in} \,\&\, (A \mid B) \mid (A \,\&\, B)$ $Sum = !C_{out} \,\&\, (A \mid B \mid C_{in}) \mid (A \,\&\, B \,\&\, C_{in})$

Transient Response

- *DC analysis* tells us V_{out} if V_{in} is constant
- *Transient analysis* tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to V_{DD} or vice versa

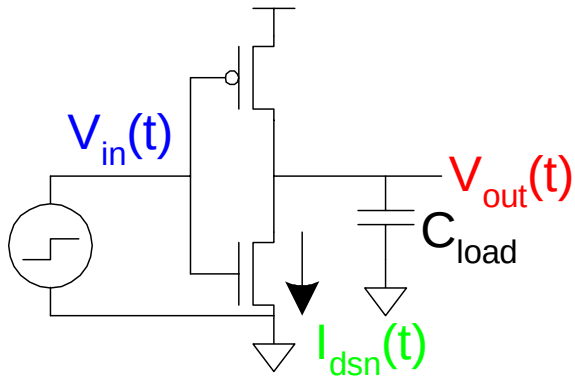
Inverter Step Response

- Ex: find step response of inverter driving load cap

$$V_{in}(t) =$$

$$V_{out}(t < t_0) =$$

$$\frac{dV_{out}(t)}{dt} =$$



Inverter Step Response

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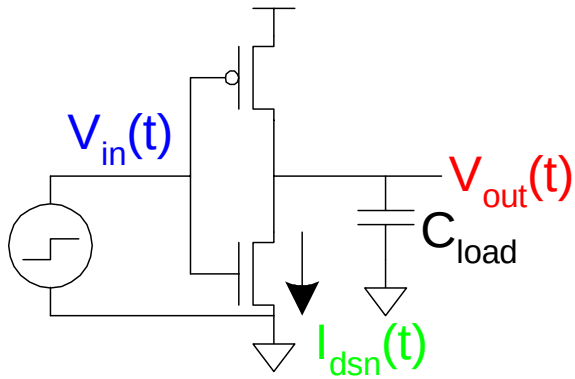

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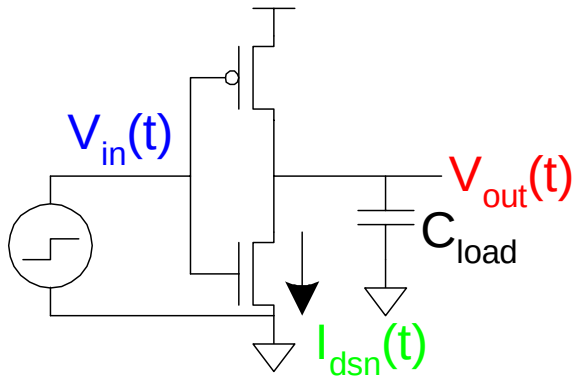

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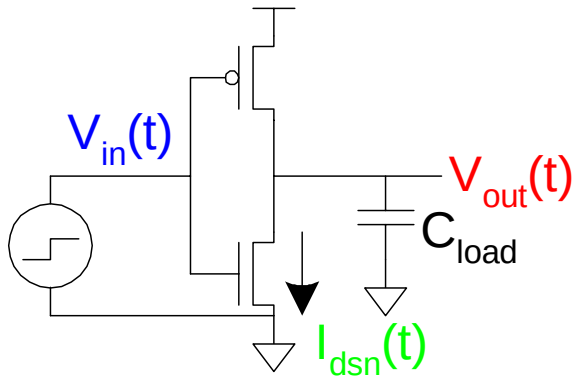

$$I_{dsn}(t) = \begin{cases} t \le t_0 \\ V_{out} > V_{DD} - V_t \\ V_{out} < V_{DD} - V_t \end{cases}$$

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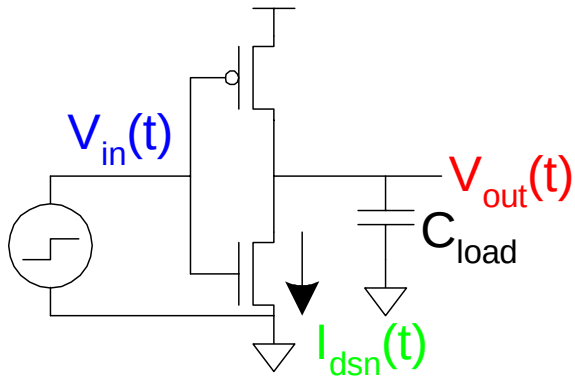

$$I_{dsn}(t) = \begin{cases} 0 & t \le t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - V_{out}(t)/2\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$

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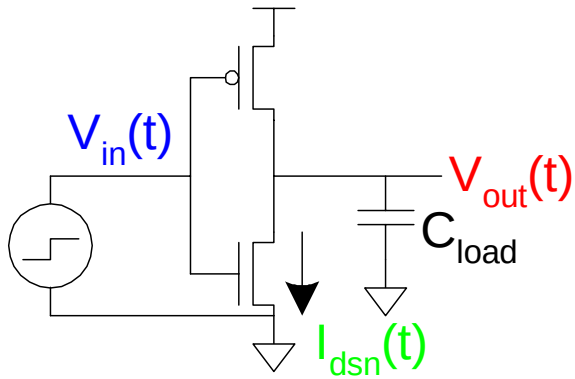

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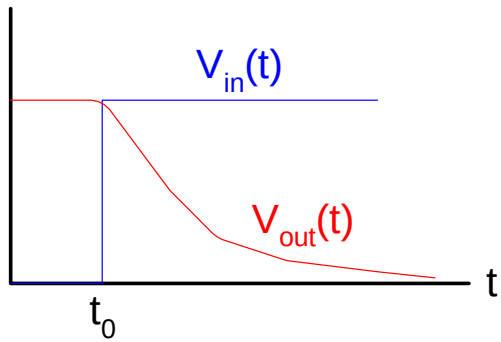


Delay Definitions

- t_{pdr}:
- t_{pdf}:
- t_{pd}:
- t_r:
- t_f: *fall time*

Delay Definitions

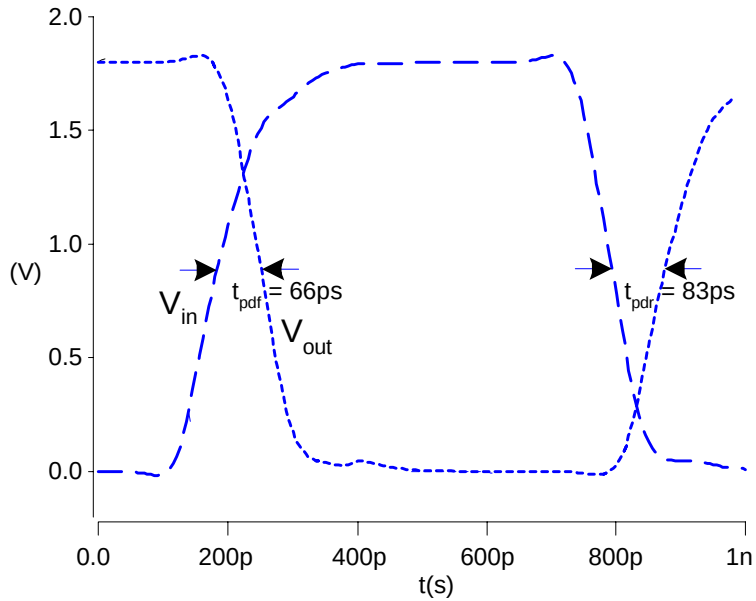
- **t_{pdr}**: *rising propagation delay*
  - From input to rising output crossing $V_{DD}/2$
- **t_{pdf}**: *falling propagation delay*
  - From input to falling output crossing $V_{DD}/2$
- **t_{pd}**: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- **t_r**: *rise time*
  - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- **t_f**: *fall time*
  - From output crossing 0.8 V_{DD} to 0.2 V_{DD}

Delay Definitions

- **t_{cdr}**: *rising contamination delay*
  - From input to rising output crossing $V_{DD}/2$
- **t_{cdf}**: *falling contamination delay*
  - From input to falling output crossing $V_{DD}/2$
- **t_{cd}**: *average contamination delay*
  - $t_{pd} = (t_{cdr} + t_{cdf})/2$

Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to write

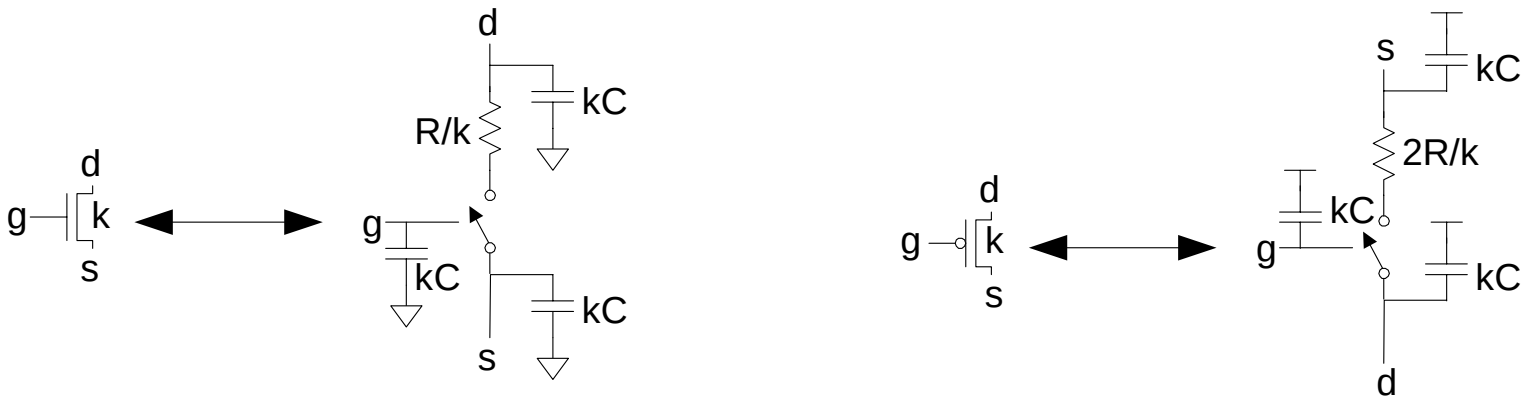


Delay Estimation

- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But easier to ask “What if?”
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use *effective resistance* R
  - So that t_{pd} = RC
- Characterize transistors by finding their effective R
  - Depends on average current as gate switches

RC Delay Models

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width



Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).

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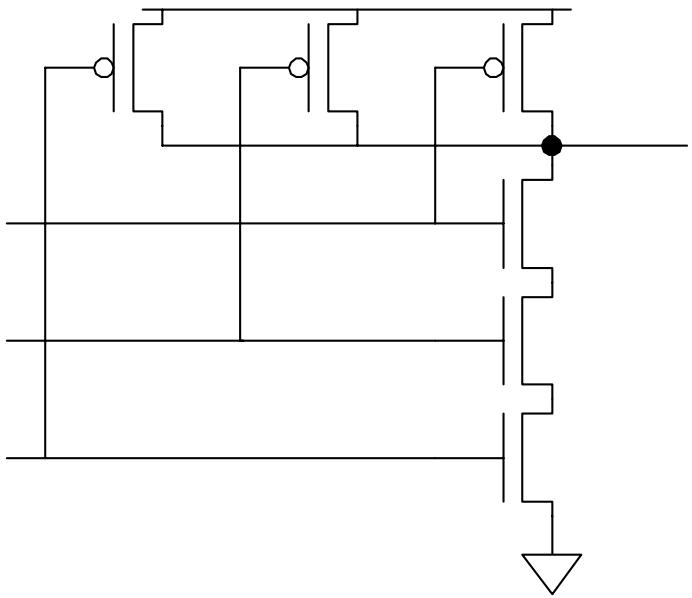

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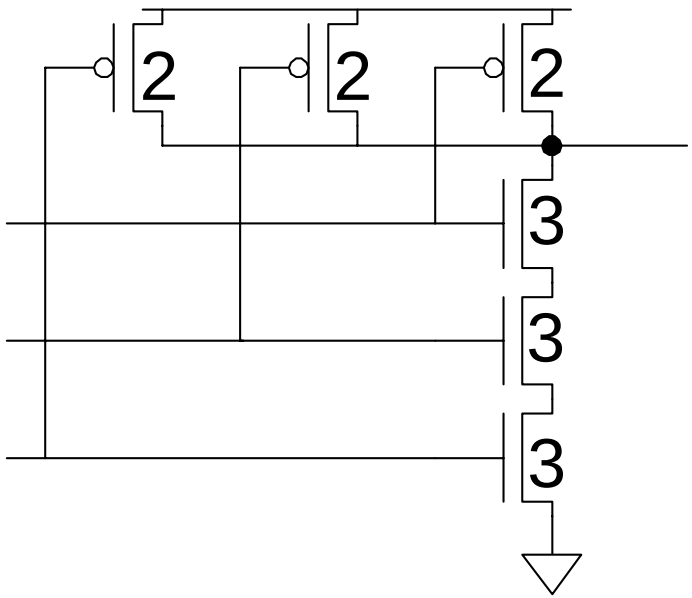
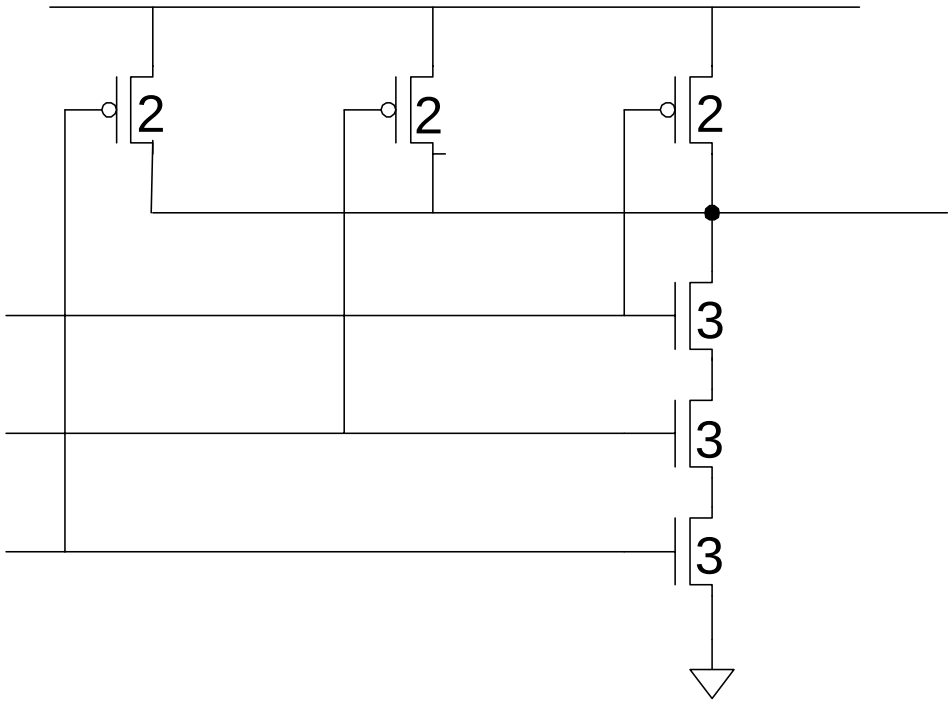


3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance.



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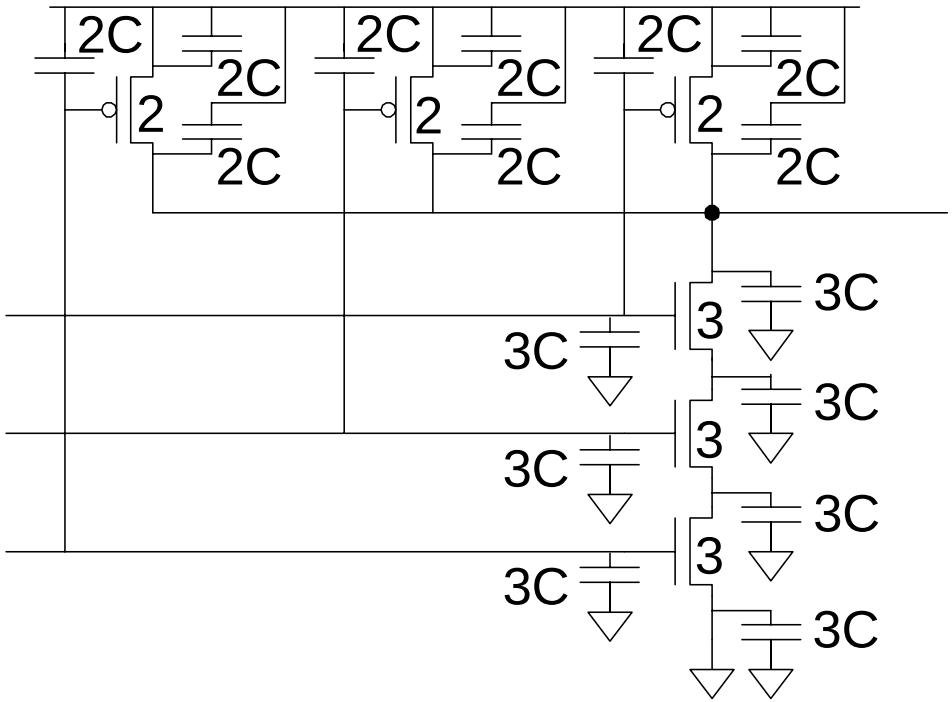

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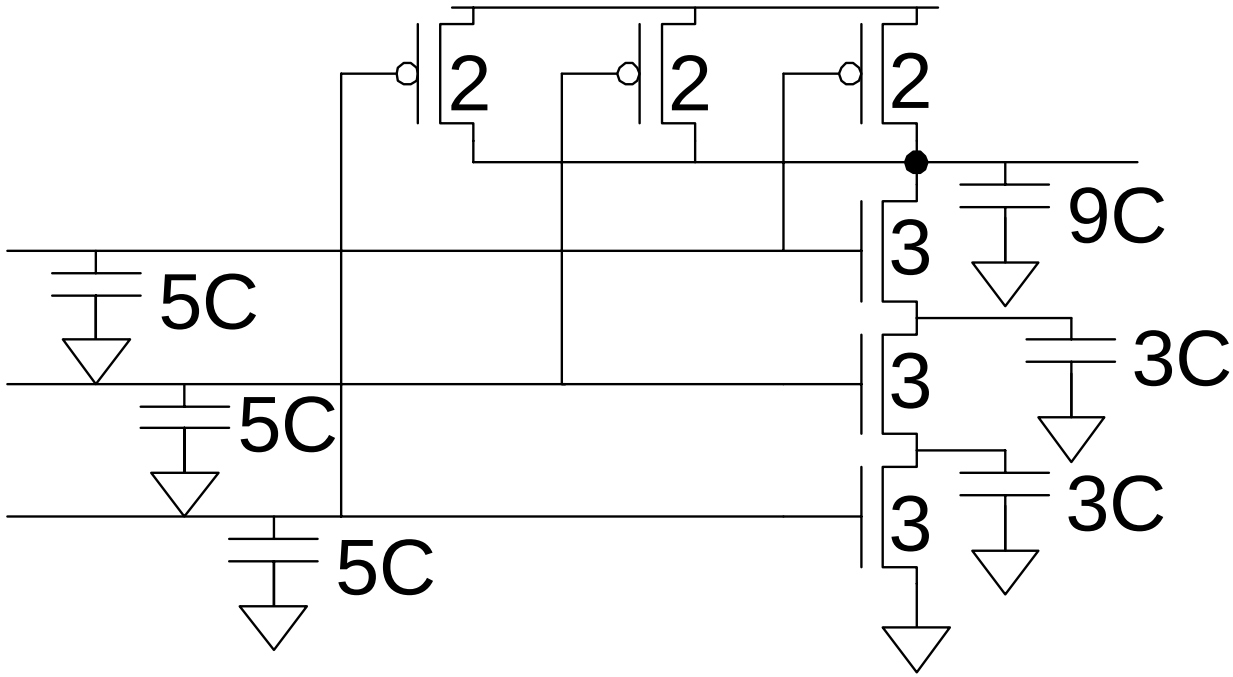
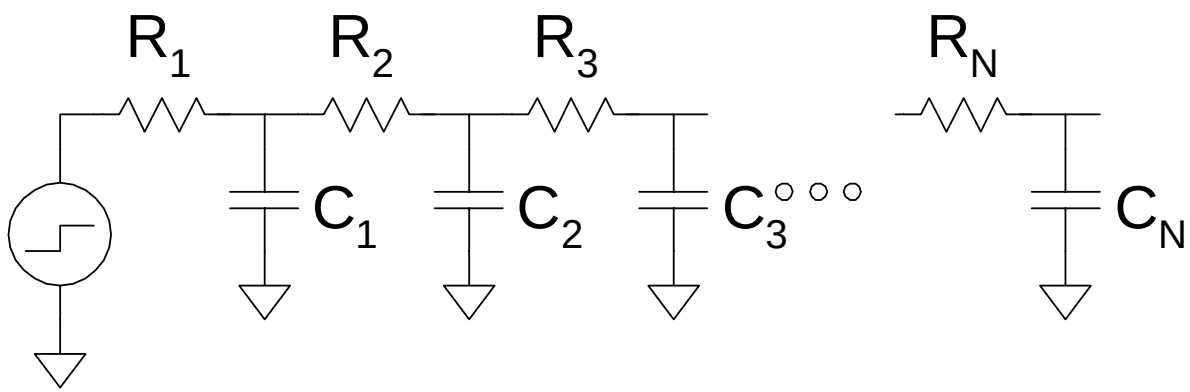


Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

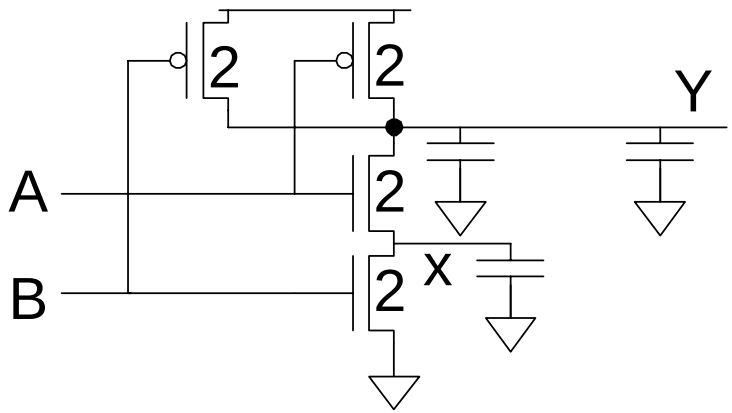
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

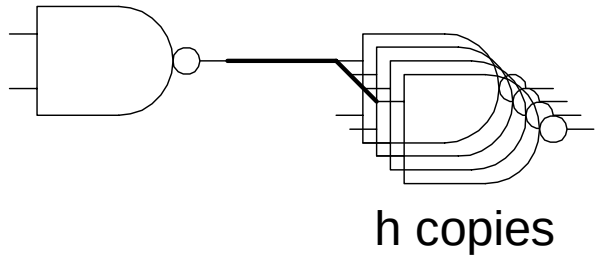
$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$



Example: 2-input NAND

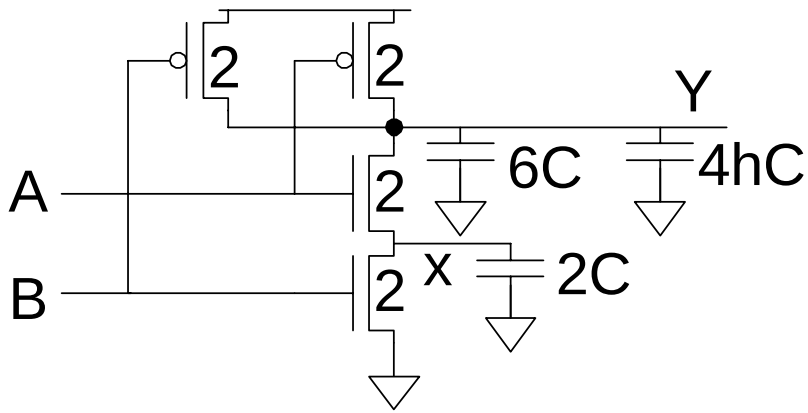
- Estimate worst-case rising and falling delay of 2-input NAND driving *h* identical gates.

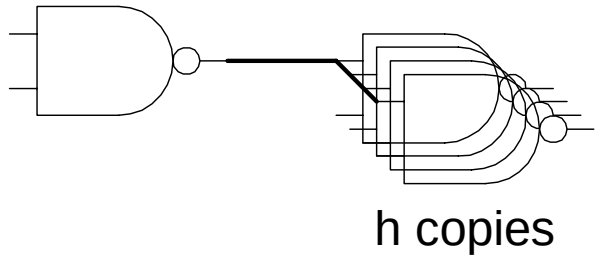




Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.





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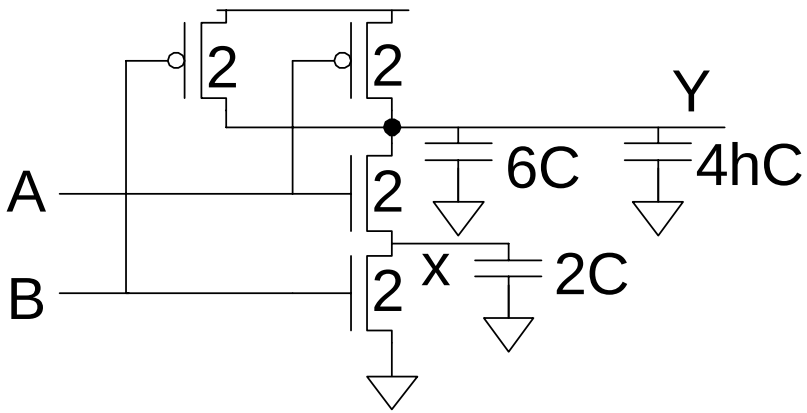

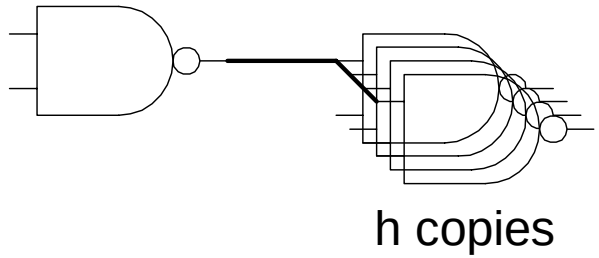

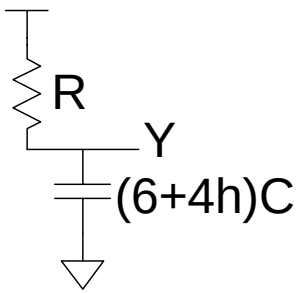

$$t_{pdr} =$$

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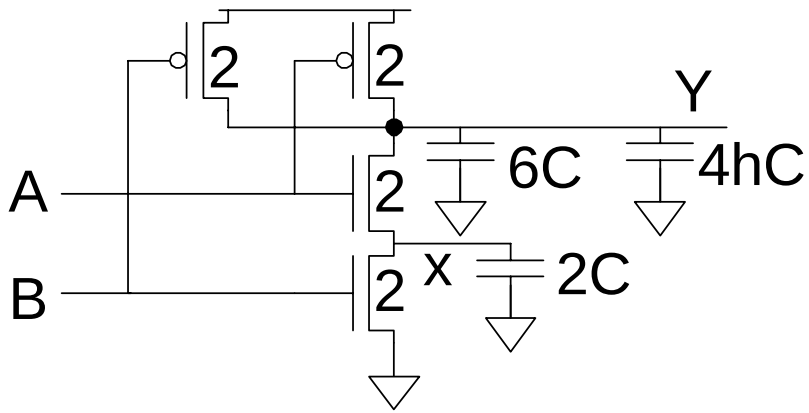

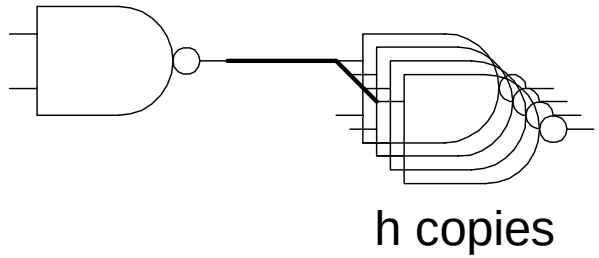

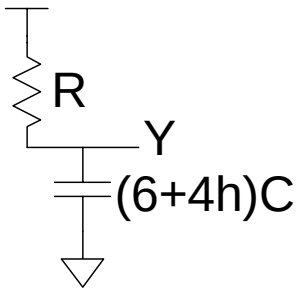

$$t_{pdr} = (6 + 4h)RC$$

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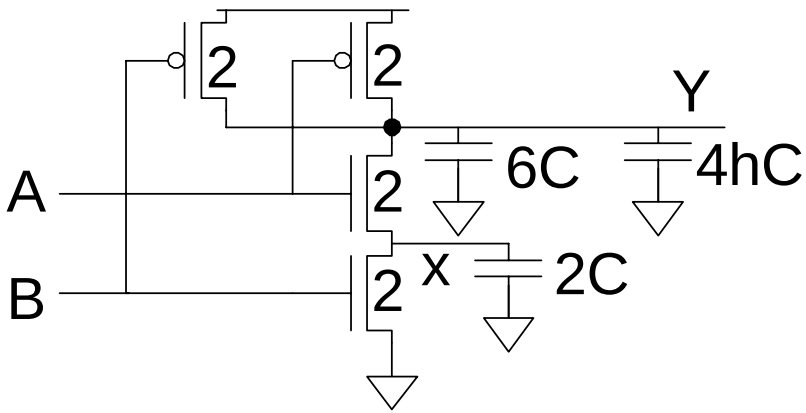

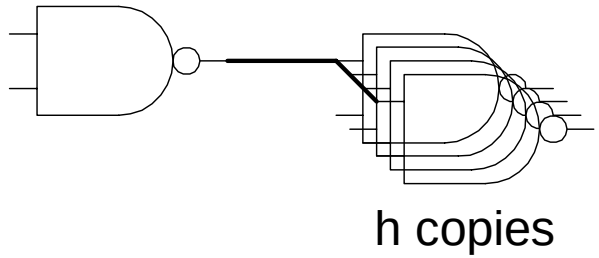

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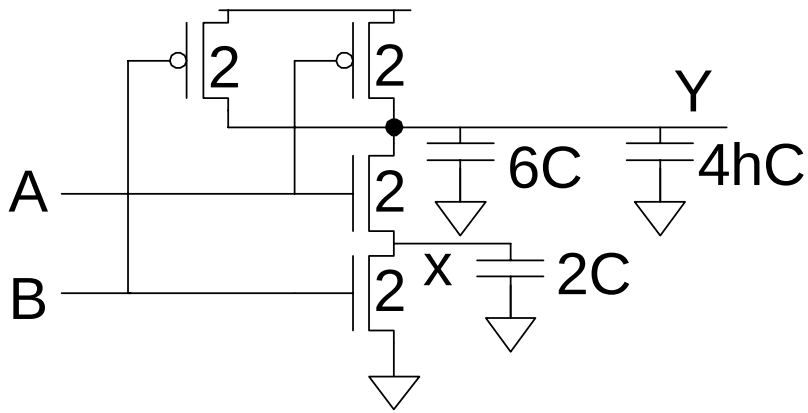

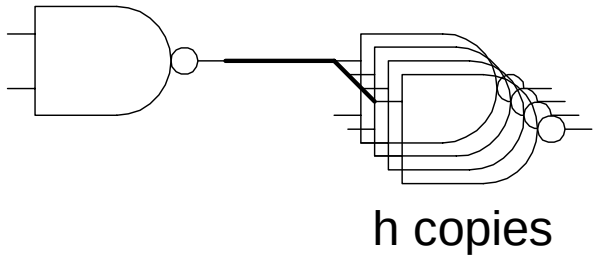

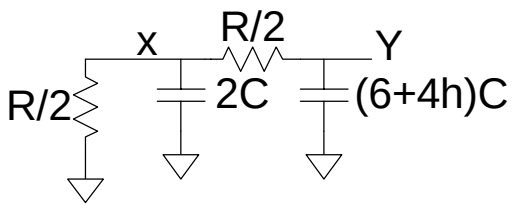

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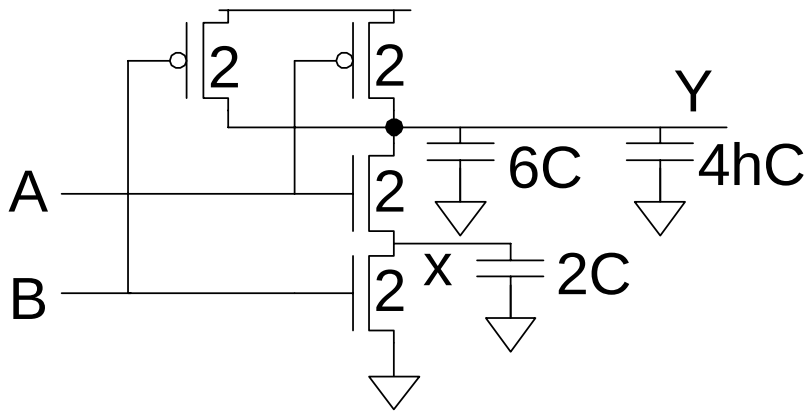
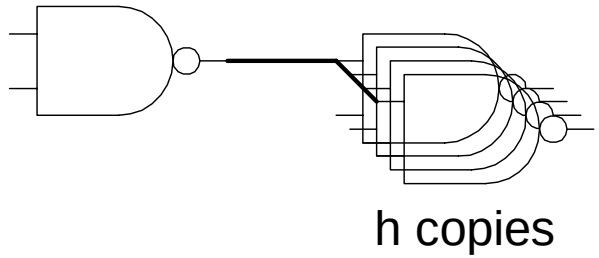
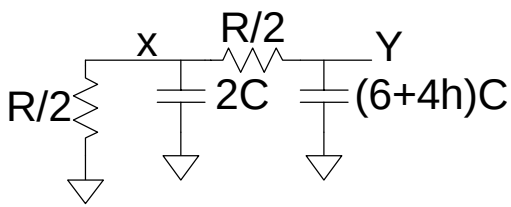






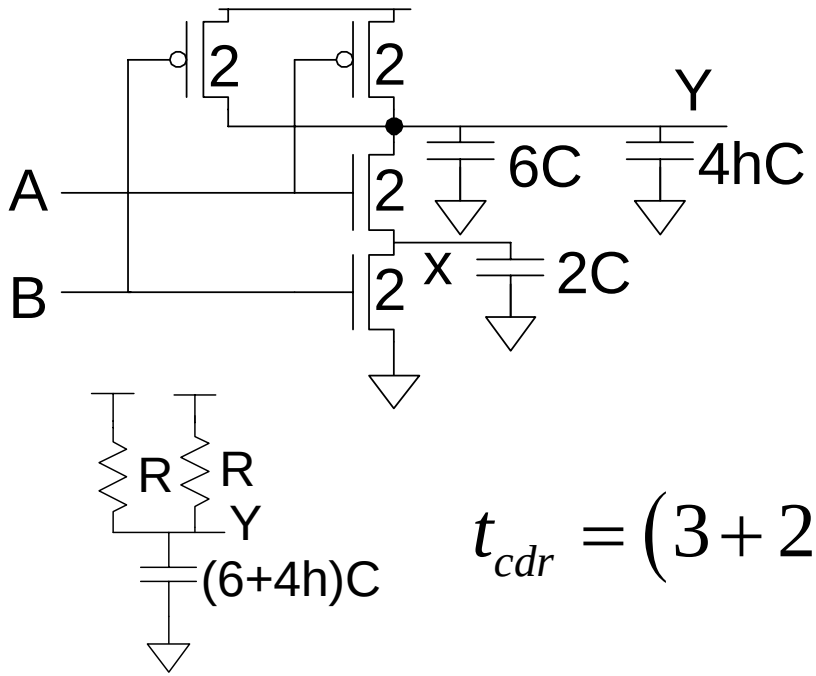
$$t_{pdf} = (2C)\left(\frac{R}{2}\right) + \left[(6+4h)C\right]\left(\frac{R}{2}+\frac{R}{2}\right)$$
$$= (7+4h)RC$$

Delay Components

- Delay has two parts
  - *Parasitic delay*
    - 6 or 7 RC
    - Independent of load
  - *Effort delay*
    - 4h RC
    - Proportional to load capacitance

Contamination Delay

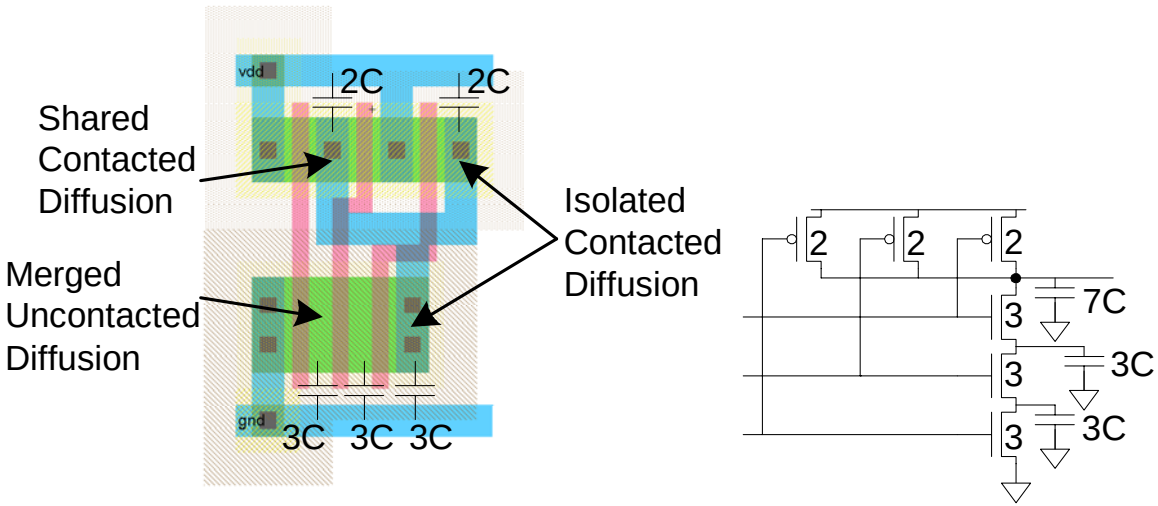
- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If both inputs fall simultaneously



$$t_{cdr} = \left(3 + 2h\right) RC$$

Diffusion Capacitance

- we assumed contacted diffusion on every s / d.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion might help too



Layout Comparison

- Which layout is better?