CPE/EE 427, CPE 527
VLSI Design I
Complementary CMOS Logic Gates

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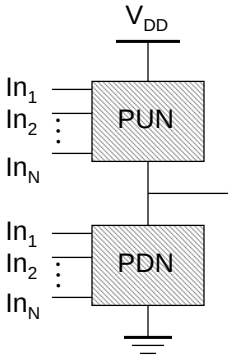
Static CMOS Logic

CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - VOH and VOL are at VDD and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between VDD and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)
- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

Static Complementary CMOS

Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

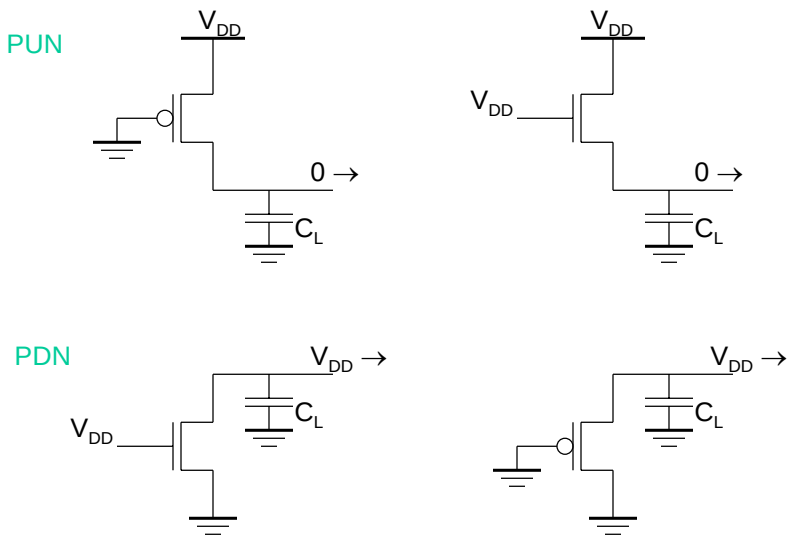
pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

NMOS transistors only

PUN and PDN are dual logic networks

Threshold Drops



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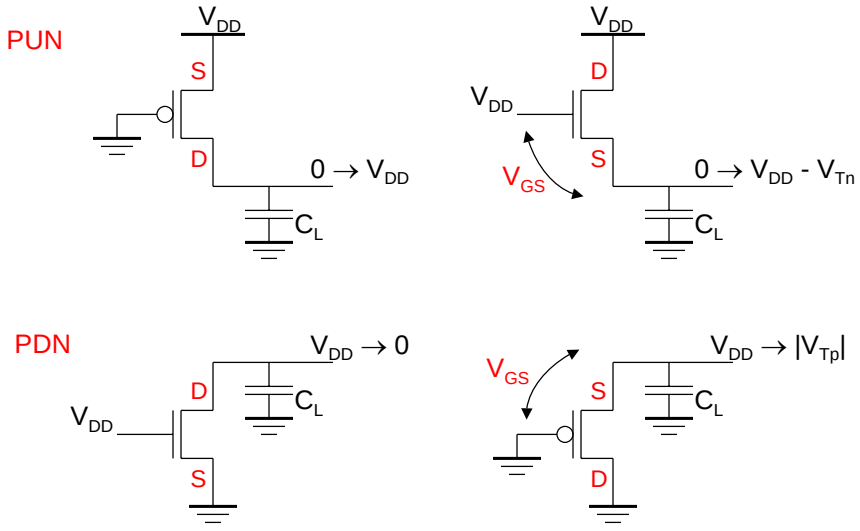
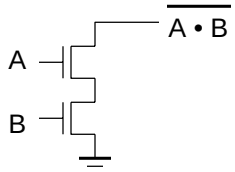
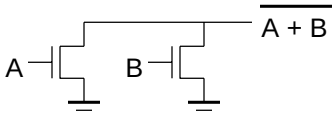


Construction of PDN

- NMOS devices in series implement a NAND function



- NMOS devices in parallel implement a NOR function



Dual PUN and PDN

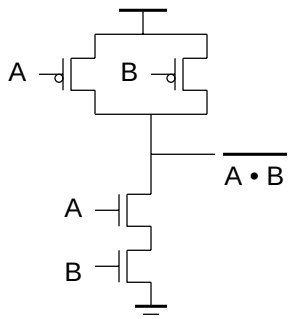
- PUN and PDN are dual networks
  - DeMorgan's theorems

$\overline{A + B} = \overline{A} \cdot \overline{B}$ [!(A + B) = !A • !B or !(A | B) = !A & !B]

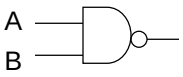
$\overline{A \cdot B} = \overline{A} + \overline{B}$ [!(A • B) = !A + !B or !(A & B) = !A | !B]

  - a parallel connection of transistors in the PUN corresponds to a series connection of the PDN
- Complementary gate is naturally inverting (NAND, NOR, AOI, OAI)
- Number of transistors for an N-input logic gate is 2N

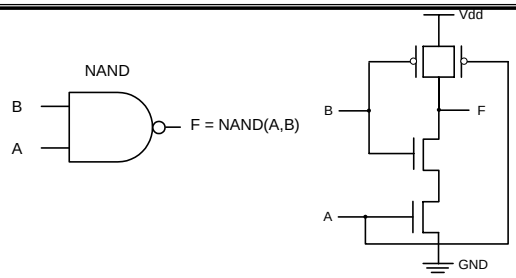
CMOS NAND

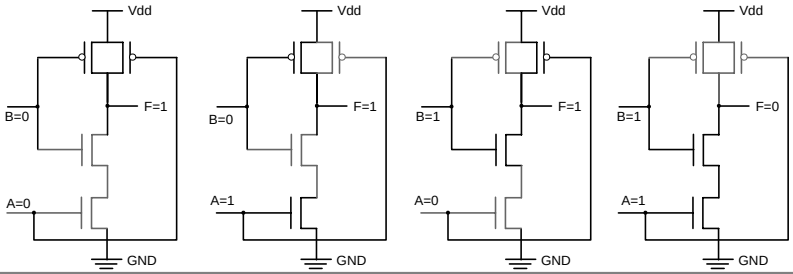


A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

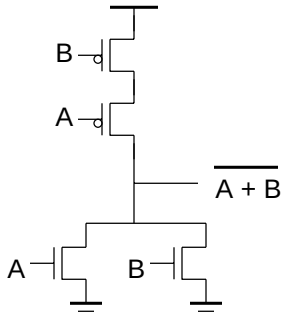


CMOS NAND





CMOS NOR



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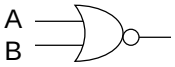
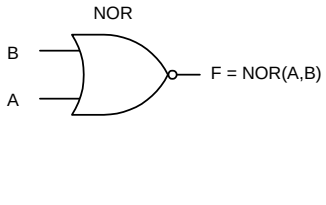
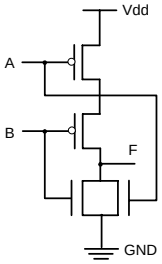
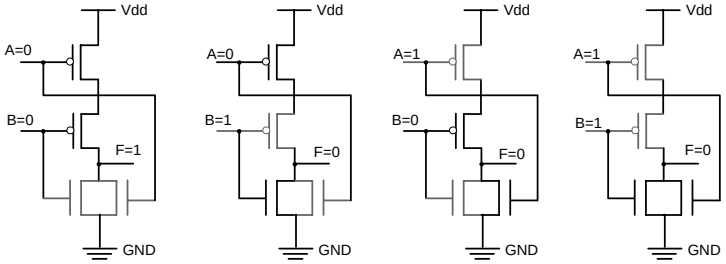


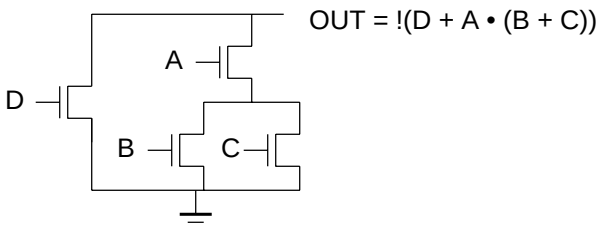
CMOS NOR







Complex CMOS Gate



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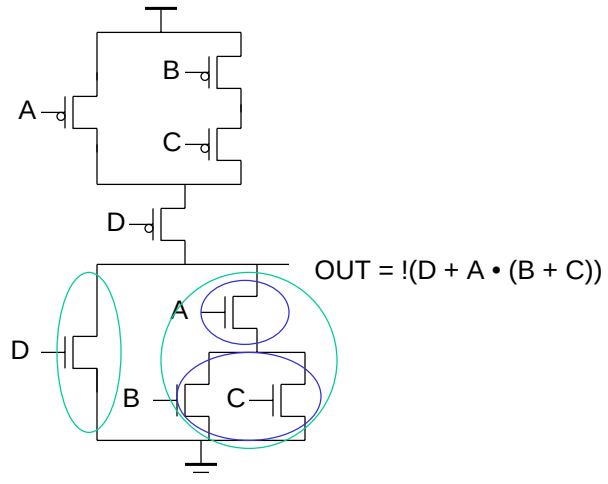
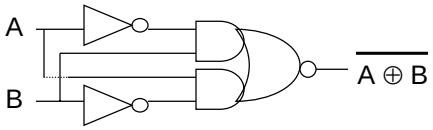
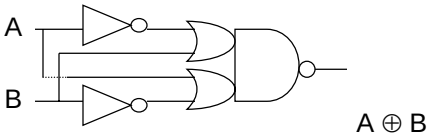


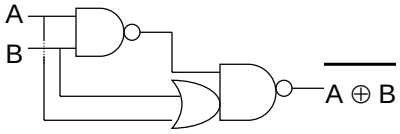
XNOR/XOR Implementation

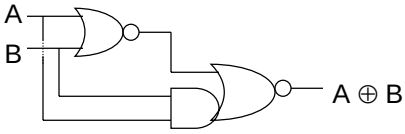
XNOR



XOR





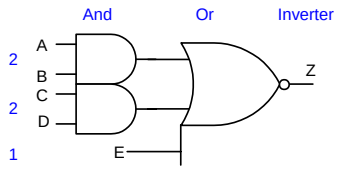


- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?

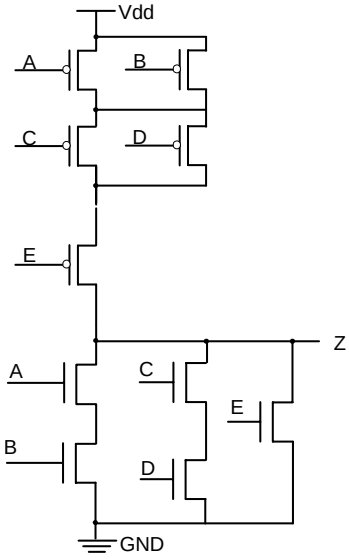
Combinational Logic Cells

- CMOS logic cells
  - AND-OR-INVERT (AOI)
  - OR-AND-INVERT(OAI)
- Example: AOI221
  Z = (A*B + C*D + E)'
  Z = AOI221(A, B, C, D, E)
  Exercise: Construct this logic cell?
- Example: OAI321
  Z = [(A+B+C)*(D+E)*F]'
  Z = OAI321(A, B, C, D, E, F)
  Exercise: Construct this logic cell?

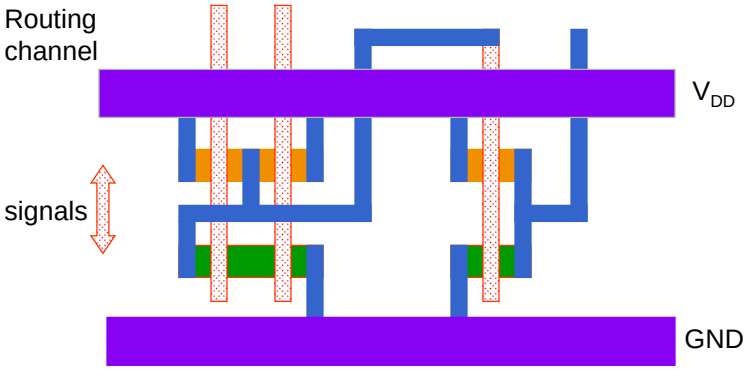
AOI221



AOI221

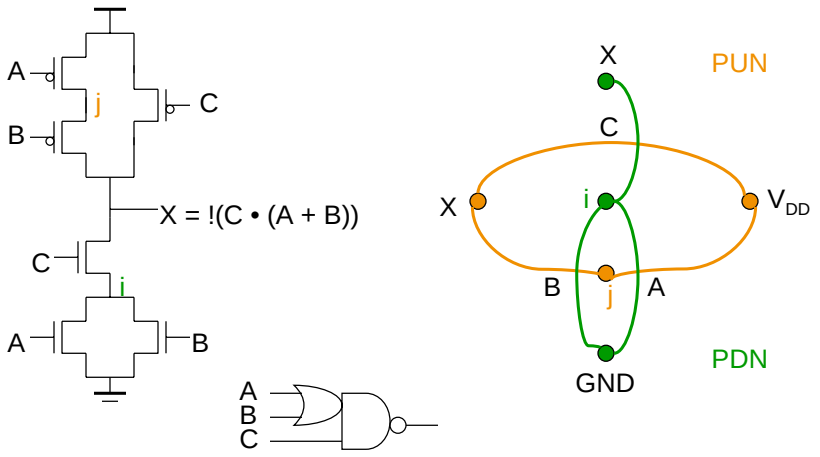


Standard Cell Layout Methodology

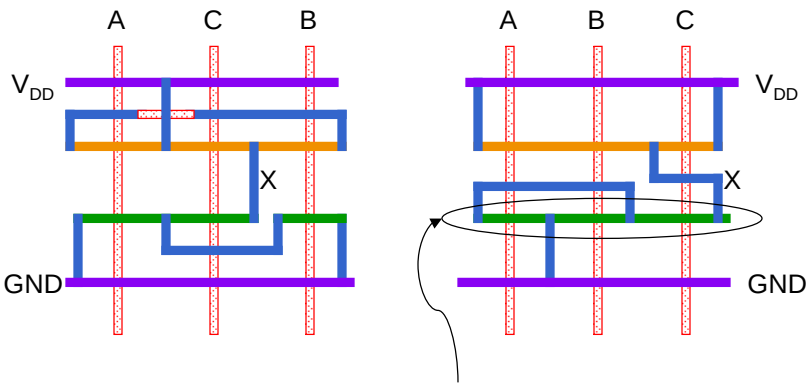


What logic function is this?

OAI21 Logic Graph

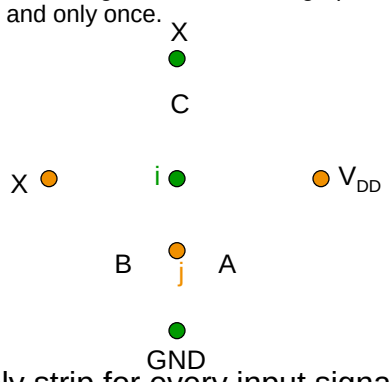


Two Stick Layouts of !(C • (A + B))



Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.



- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

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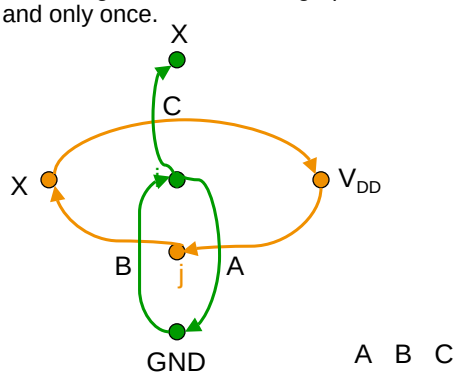

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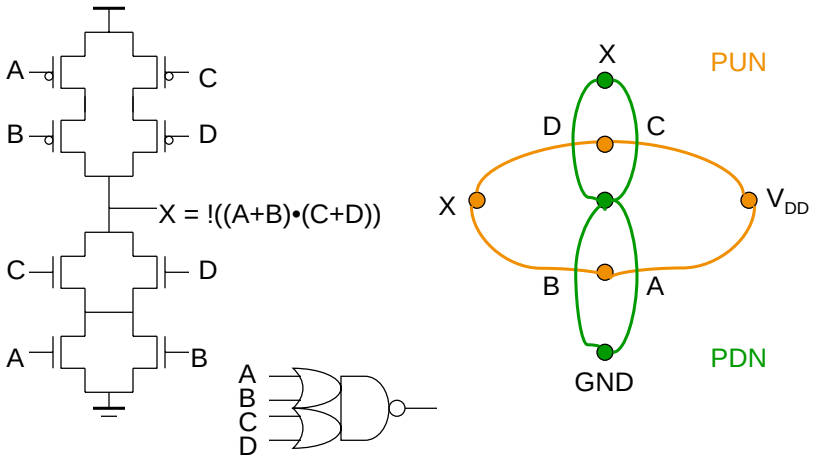
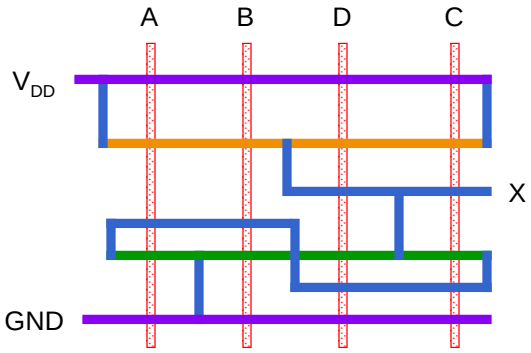
OAI22 Logic Graph



OAI22 Layout



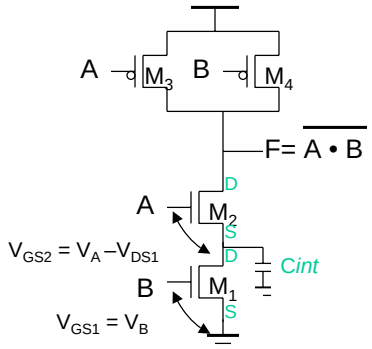
- Some functions have no consistent Euler path like x = !(a + bc + de) (but x = !(bc + a + de) does!)

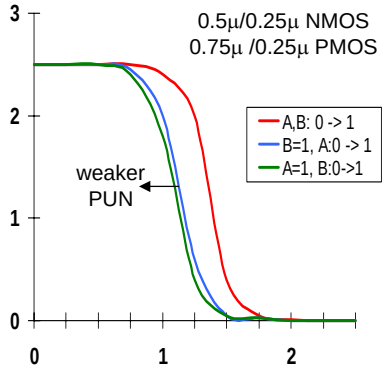
Combinational Logic Cells (cont'd)

- The AOI family of cells with 3 index numbers or less
  - X = {AOI, OAI, AO, OA}; a,b,c={2,3}

Cell Type	Cells	Number of Unique Cells
Xa1	X21, X31	2
Xa11	X211, X311	2
Xab	X22, X33, X32	3
Xab1	X221, X321, X331	3
Xabc	X222, X333, X332, X322	4
Total		**14**

VTC is Data-Dependent





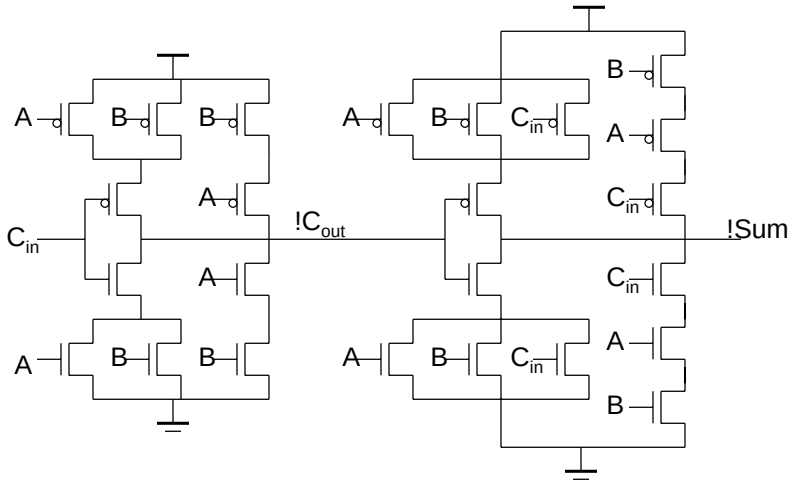
- The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

$V_{Tn1} = V_{Tn0}$

$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{(|2\phi_F| + V_{int})} - \sqrt{|2\phi_F|})$

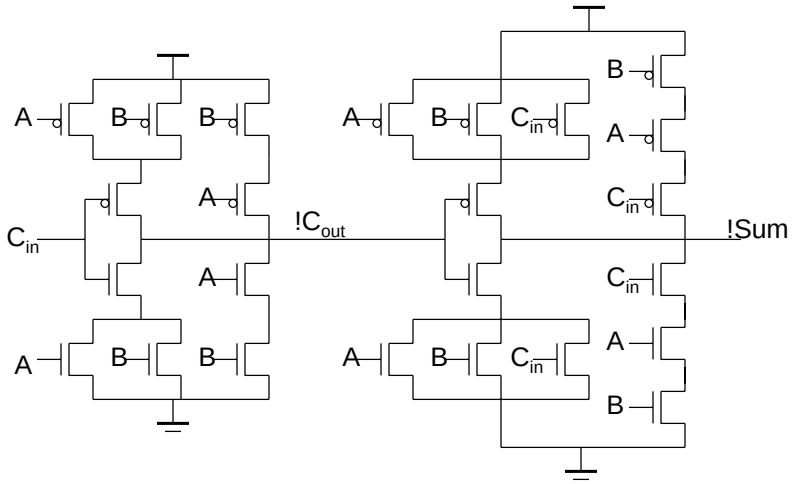
since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of C*int*

Static CMOS Full Adder Circuit



Static CMOS Full Adder Circuit

$!C_{out} = !C_{in}$ & (!A | !B) | (!A & !B) $!Sum = C_{out}$ & (!A | !B | $!C_{in}$) | (!A & !B & $!C_{in}$)



$C_{out} = C_{in}$ & (A | B) | (A & B) Sum = $!C_{out}$ & (A | B | C_{in}) | (A & B & C_{in})