CPE/EE 427, CPE 527
VLSI Design I
IC Manufacturing

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University of Alabama in Huntsville

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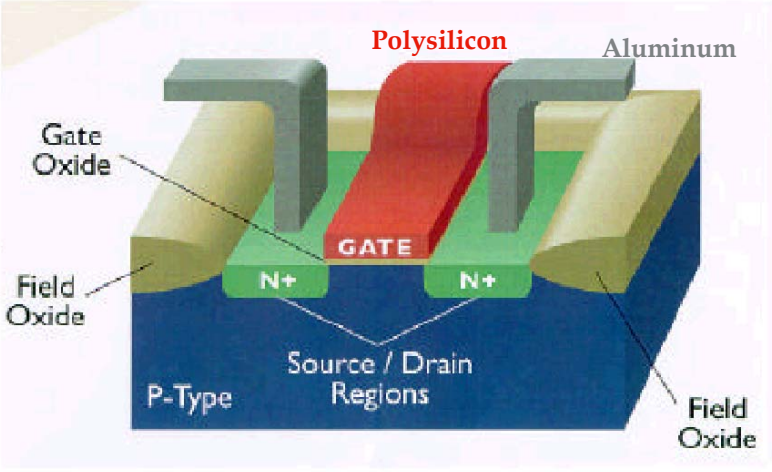
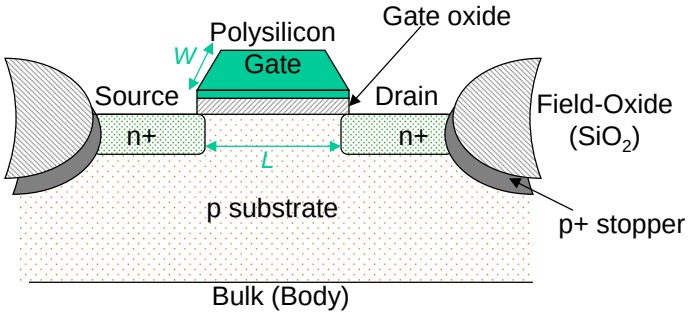
The MOS Transistor



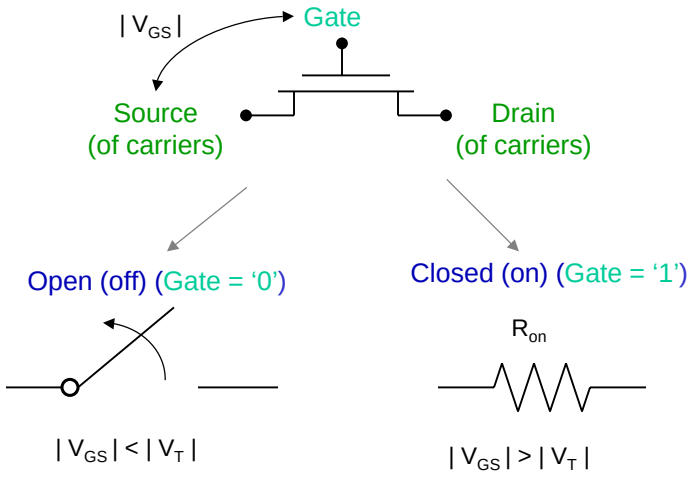
The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration N_D - electrons are the majority carriers

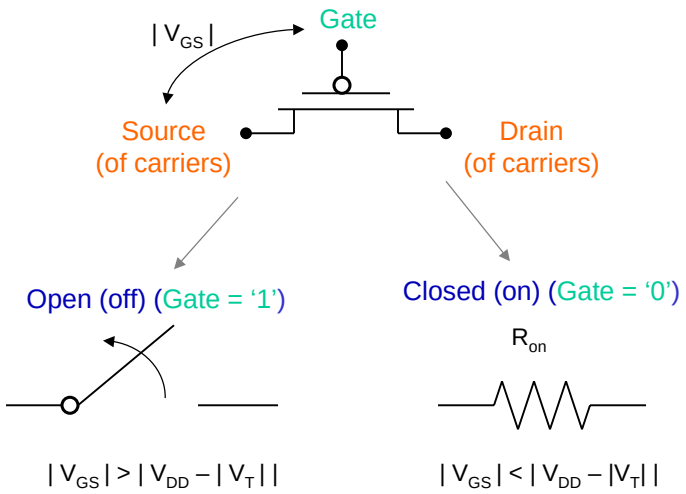


p areas have been doped with acceptor ions (boron) of concentration N_A - holes are the majority carriers

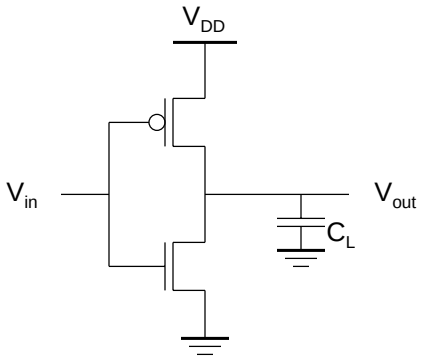
Switch Model of NMOS Transistor



Switch Model of PMOS Transistor

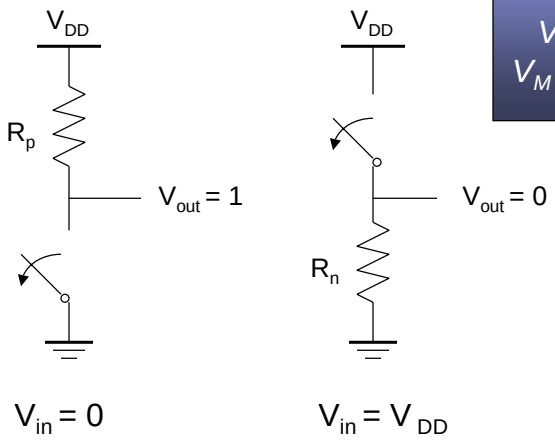


CMOS Inverter:
A First Look



CMOS Inverter:
Steady State Response

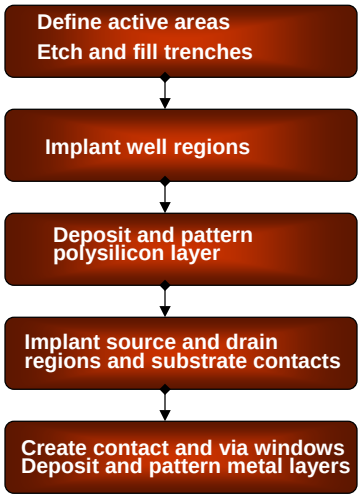
$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$



Growing the Silicon Ingot

From *Smithsonian*, 2000

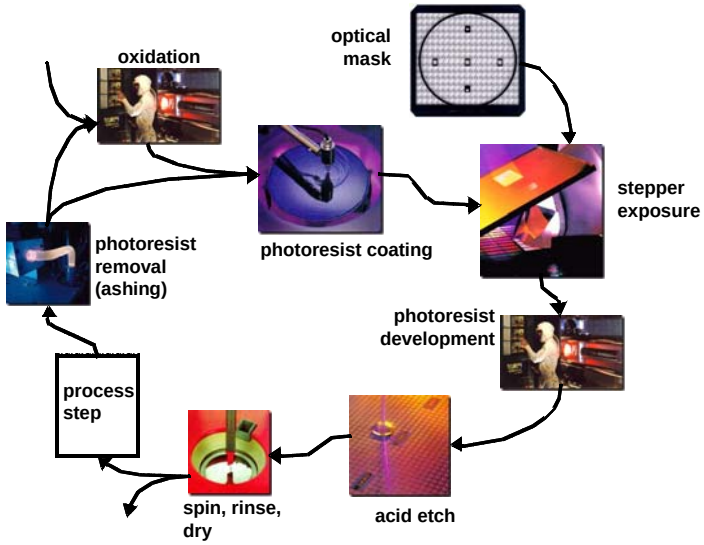
CMOS Process at a Glance



- One full photolithography sequence per layer (mask)
- Built (roughly) from the bottom up
  - 5 metal 2
  - 4 metal 1
  - 2 polysilicon
  - 3 source and drain diffusions
  - 1 tubs (aka wells, active areas)

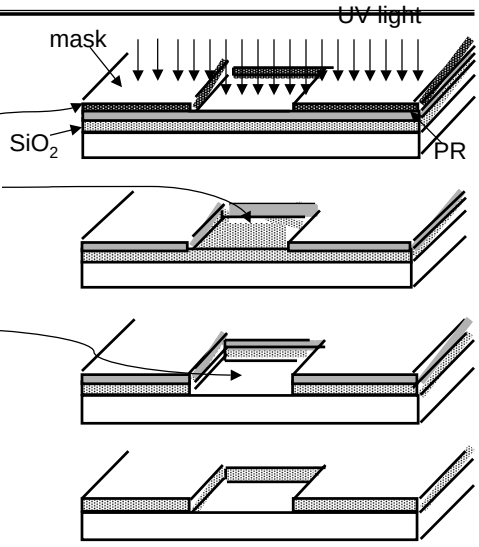
exception!

Photolithographic Process

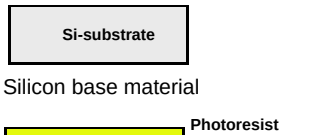


Patterning - Photolithography

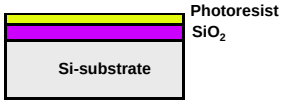
1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
   - Unexposed (negative PR)
   - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
   - Ion implantation
   - Plasma etching
   - Metal deposition
8. Photoresist removal (ashing)



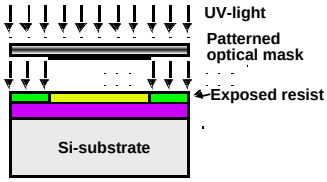
Example of Patterning of SiO2



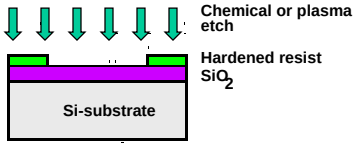
Silicon base material



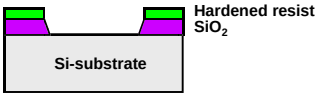
1&2. After oxidation and deposition of negative photoresist



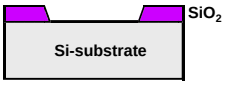
3. Stepper exposure



4. After development and etching of resist, chemical or plasma etch of SiO_2



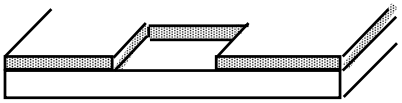
5. After etching



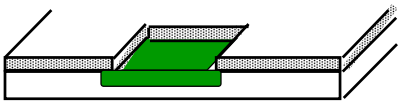
8. Final result after removal of resist

Diffusion and Ion Implantation

1. Area to be doped is exposed (photolithography)

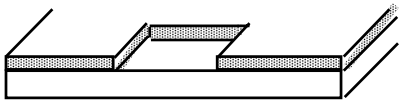


2. Diffusion
   or
   Ion implantation

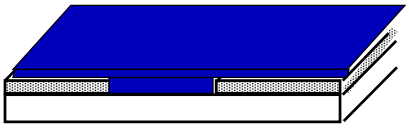


Deposition and Etching

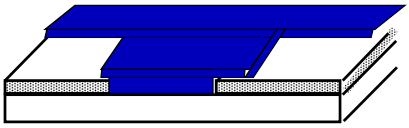
1. Pattern masking (photolithography)



2. Deposit material over entire wafer
   - CVD (Si_3N_4)
   - chemical deposition (polysilicon)
   - sputtering (Al)



3. Etch away unwanted material
   - wet etching
   - dry (plasma) etching

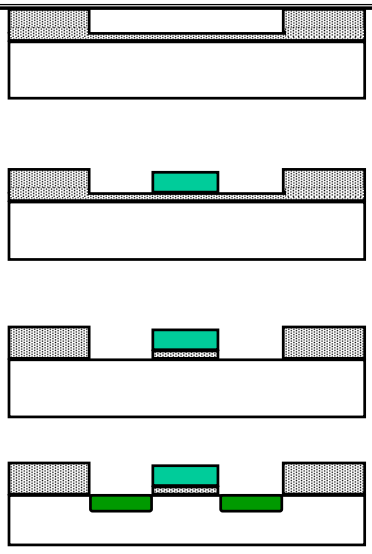


Planarization: Polishing the Wafers

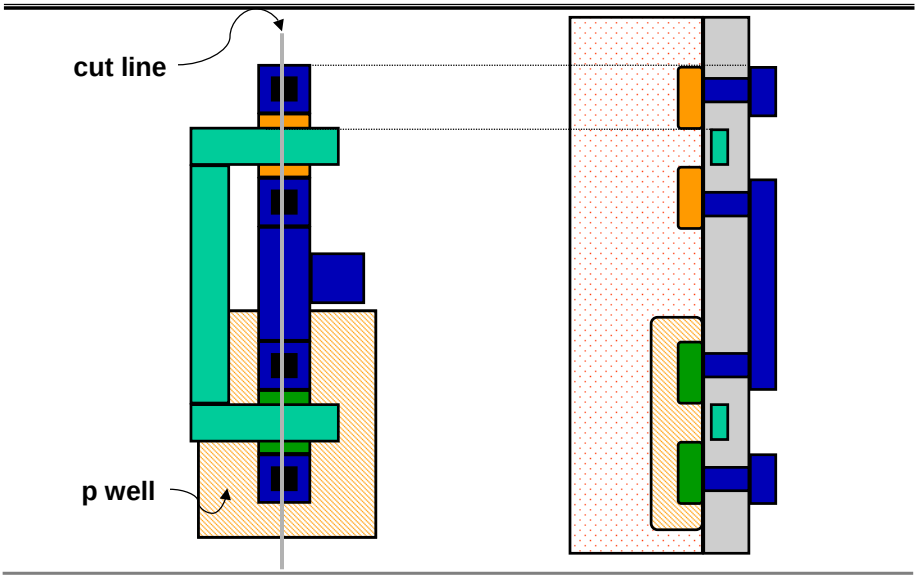
From *Smithsonian*, 2000

Self-Aligned Gates

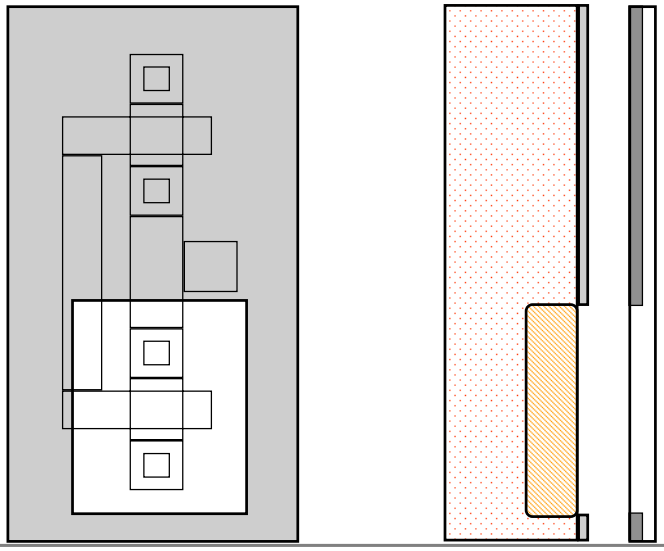
1. Create thin oxide in the "active" regions, thick elsewhere
2. Deposit polysilicon
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)
4. Implant dopant



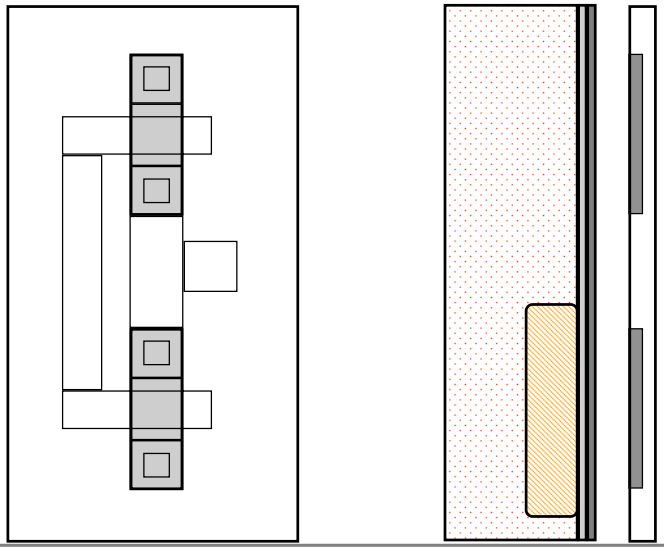
Simplified CMOS Inverter Process



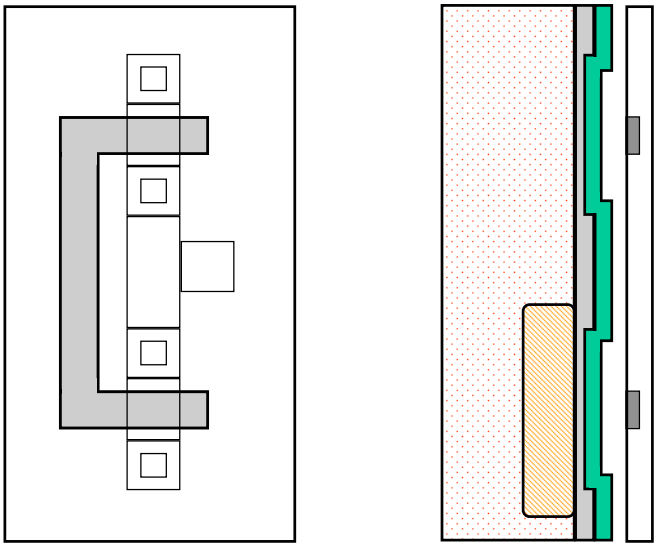
P-Well Mask



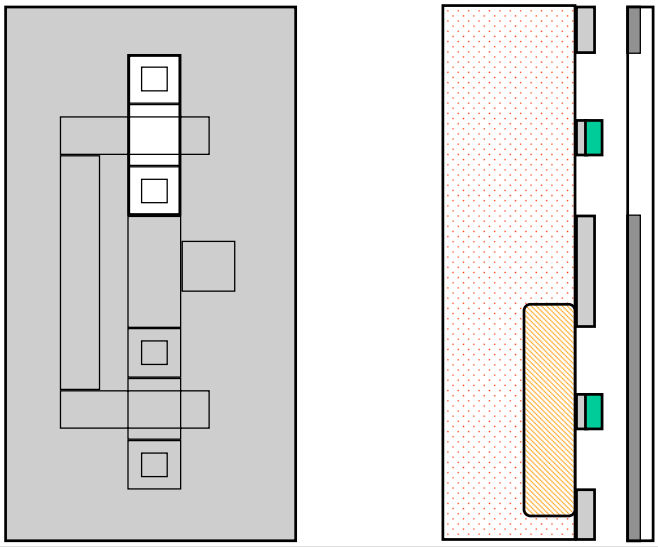
Active Mask



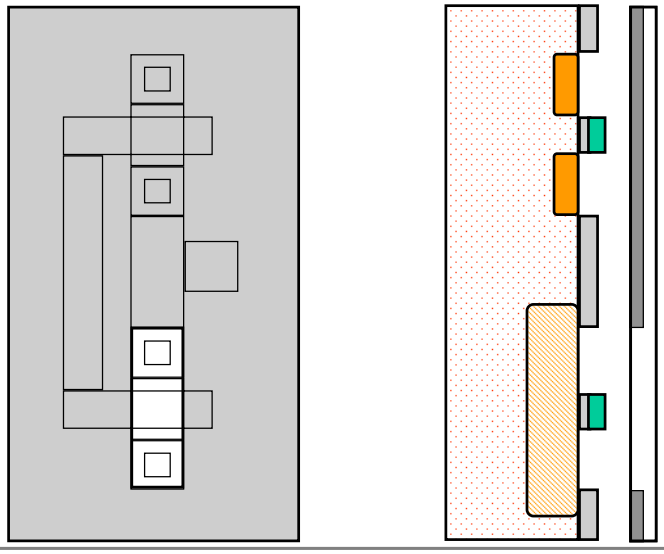
Poly Mask



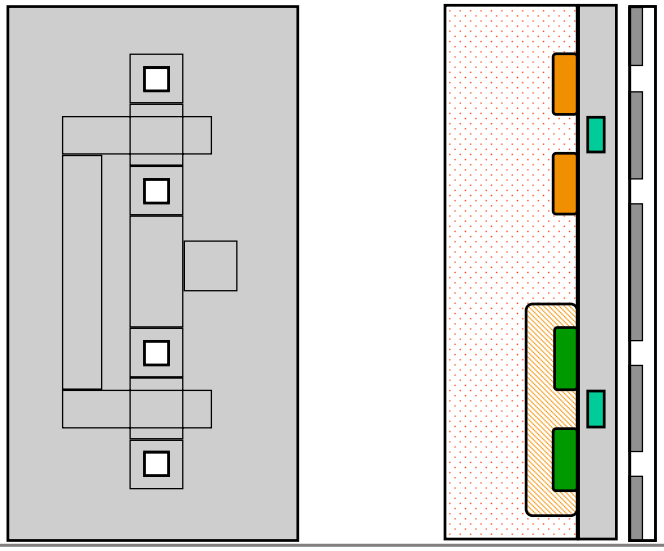
P+ Select Mask



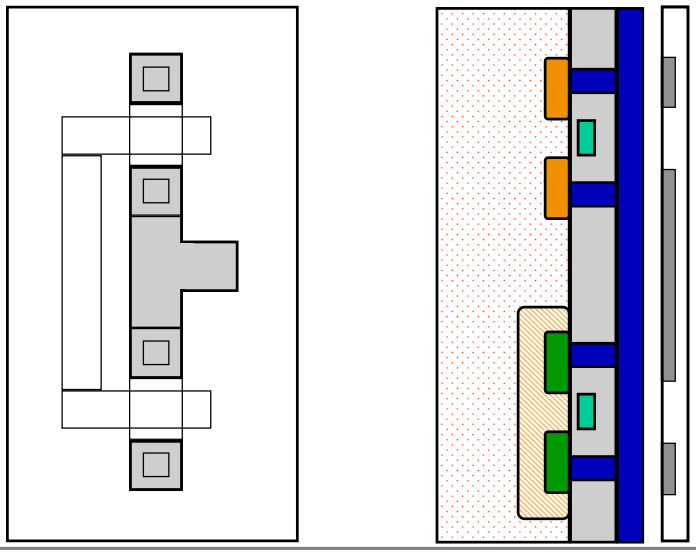
N+ Select Mask



Contact Mask

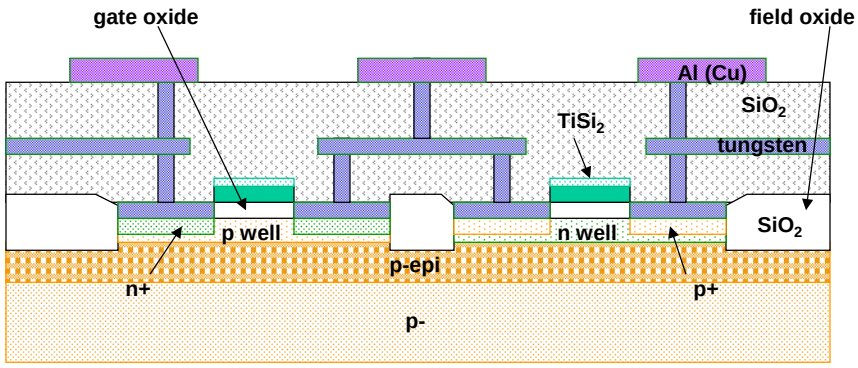


Metal Mask

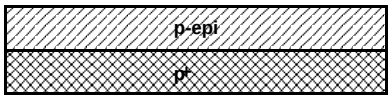


A Modern CMOS Process

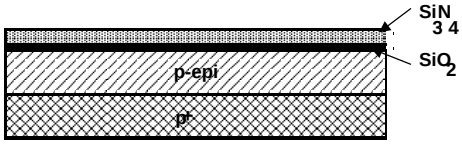
Dual-Well Trench-Isolated CMOS



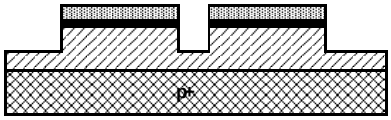
Modern CMOS Process Walk-Through



Base material: p+ substrate with p-epi layer

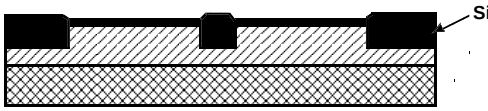


After deposition of gate-oxide and sacrifical nitride (acts as a buffer layer)

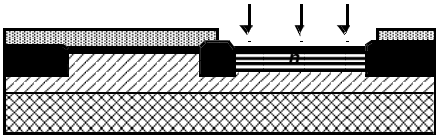


After plasma etch of insulating trenches using the inverse of the active area mask

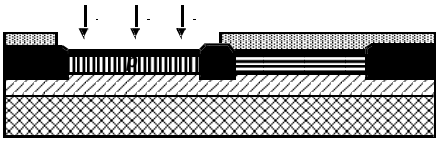
CMOS Process Walk-Through, con't



After trench filling, CMP planarization, and removal of sacrificial nitride

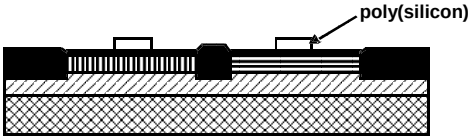


After n-well and V_{Tp} adjust implants

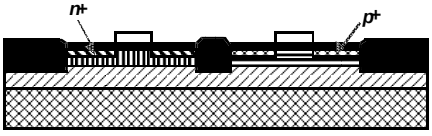


After p-well and V_{Tn} adjust implants

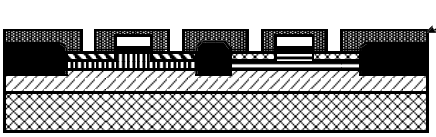
CMOS Process Walk-Through, con't



After polysilicon deposition and etch

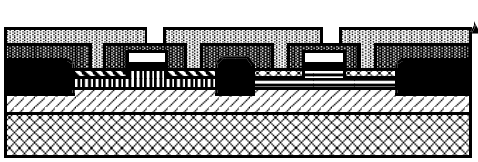


After n+ source/dram and p+ source/drain implants. These steps also dope the polysilicon.

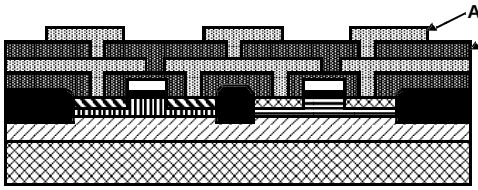


After deposition of SiO_2 insulator and contact hole etch

CMOS Process Walk-Through, con't



After deposition and patterning of first Al layer.



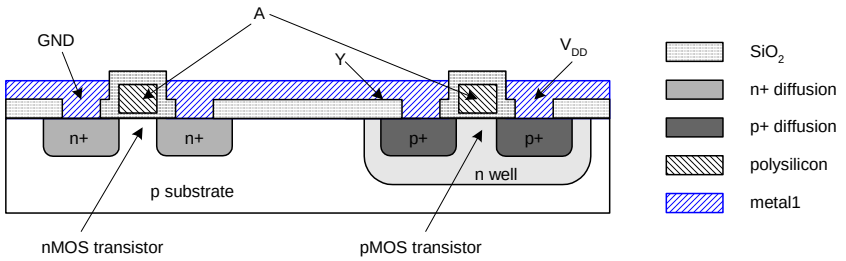
After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

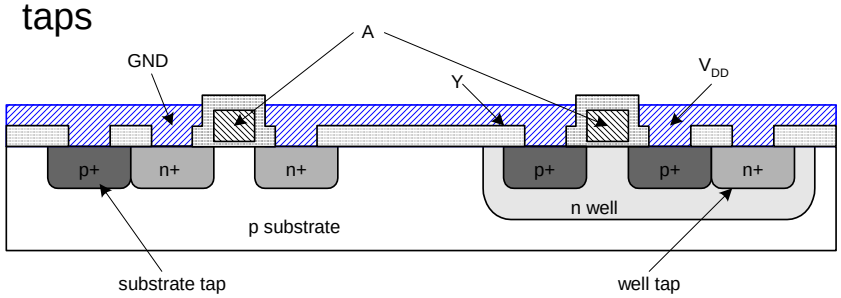
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



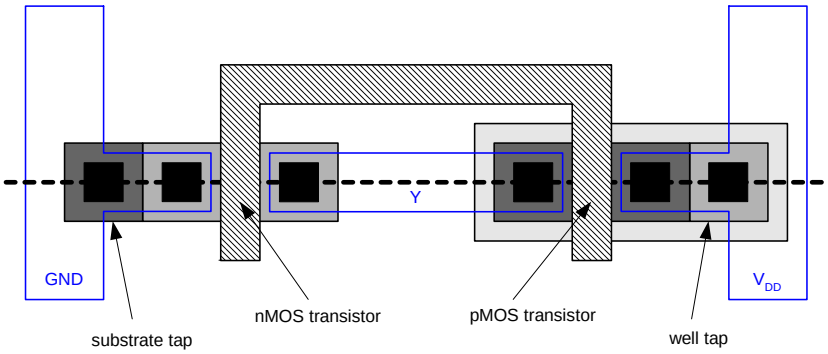
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



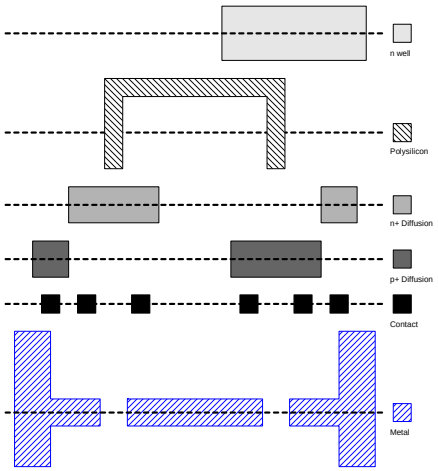
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

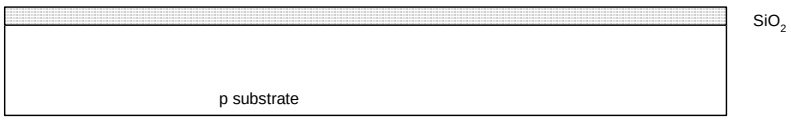


Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

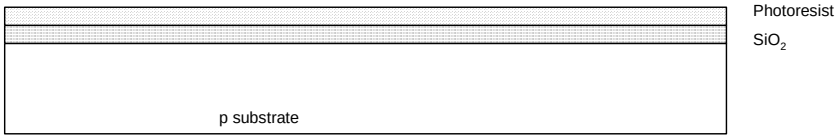
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



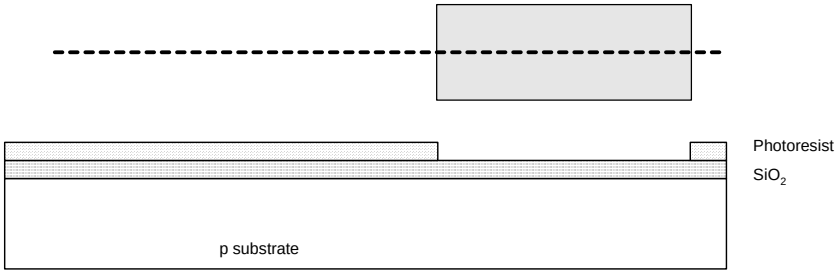
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



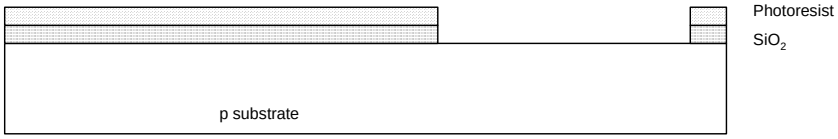
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



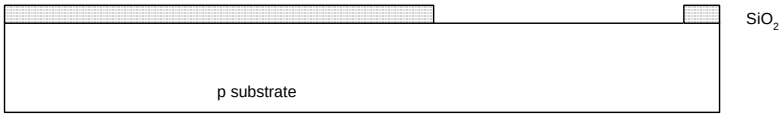
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



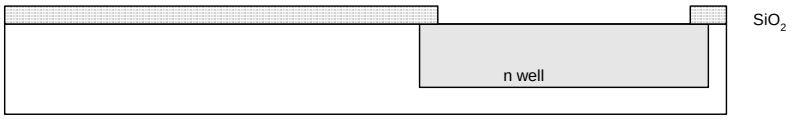
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

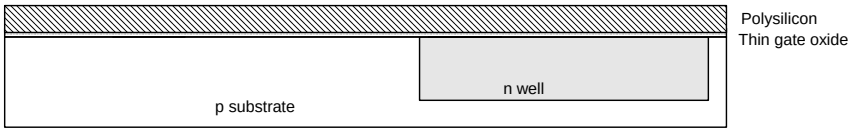


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

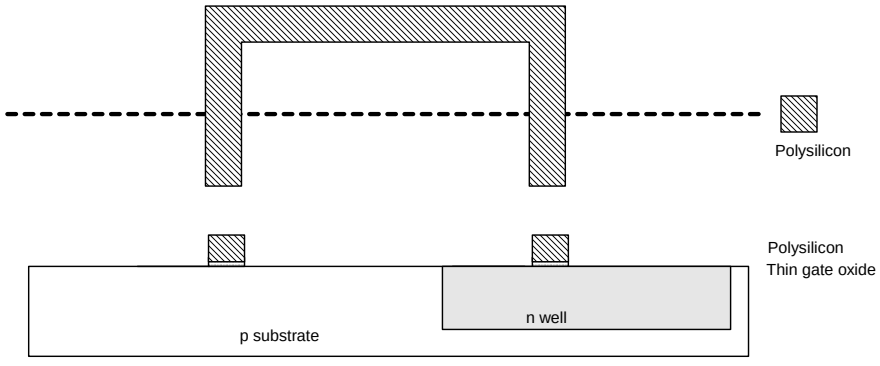
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



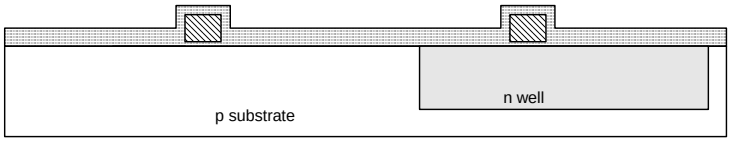
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



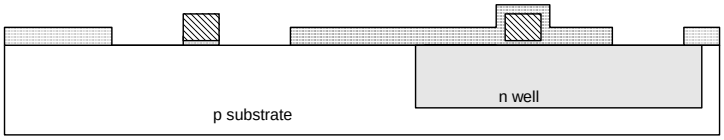
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



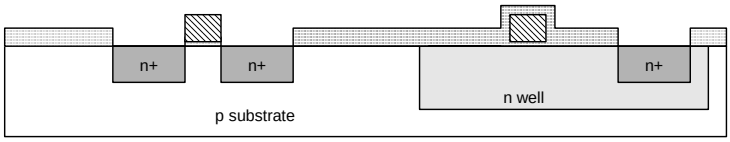
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



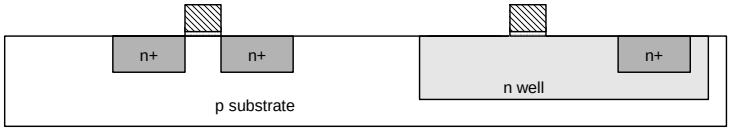
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



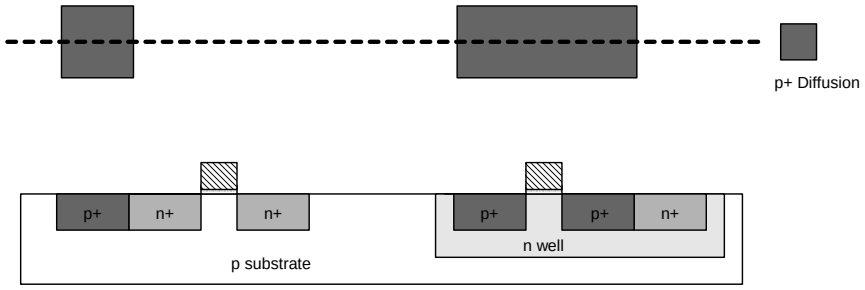
N-diffusion cont.

- Strip off oxide to complete patterning step



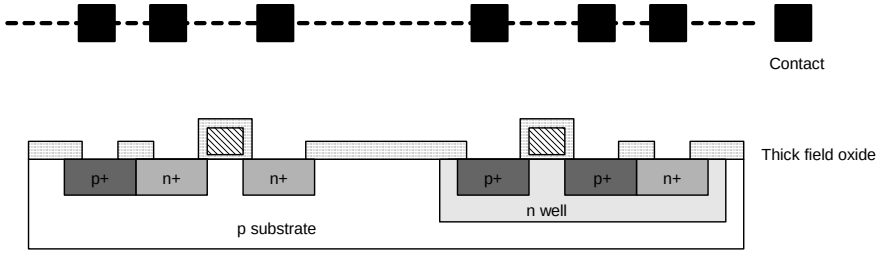
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



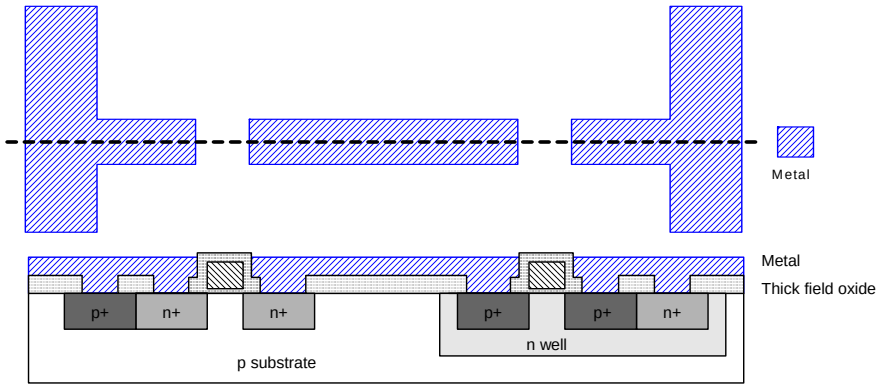
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

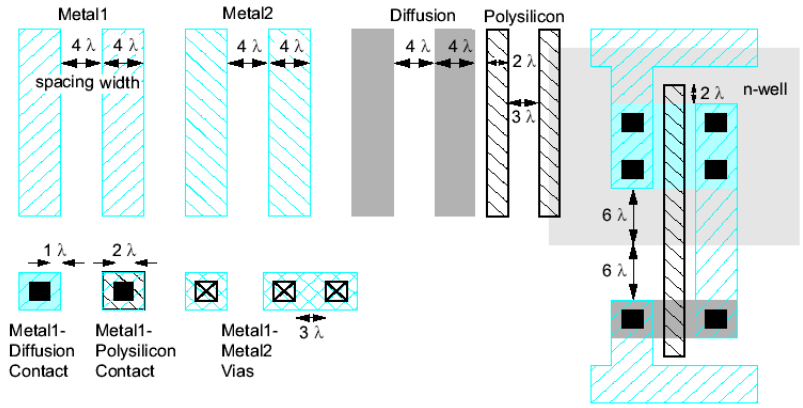


Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

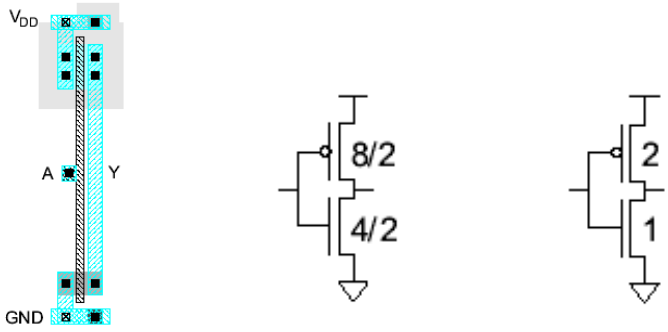
Simplified Design Rules

- Conservative rules to get you started

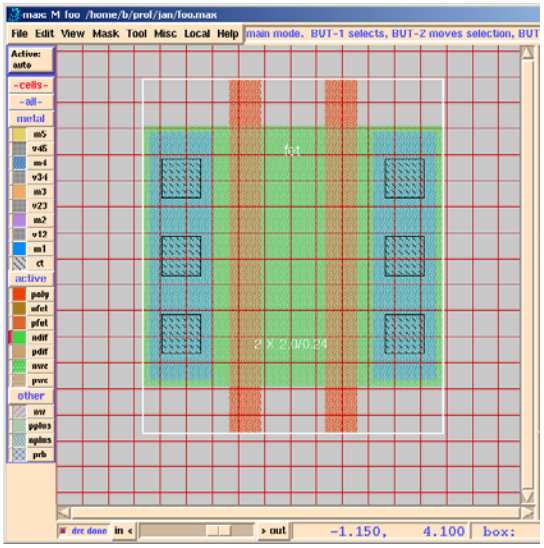


Inverter Layout

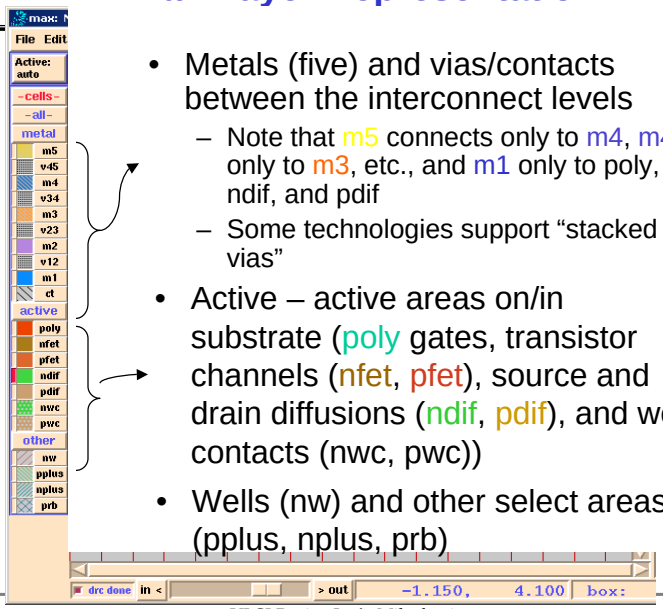
- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In *f* = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long



Layout Editor: *max* Design Frame

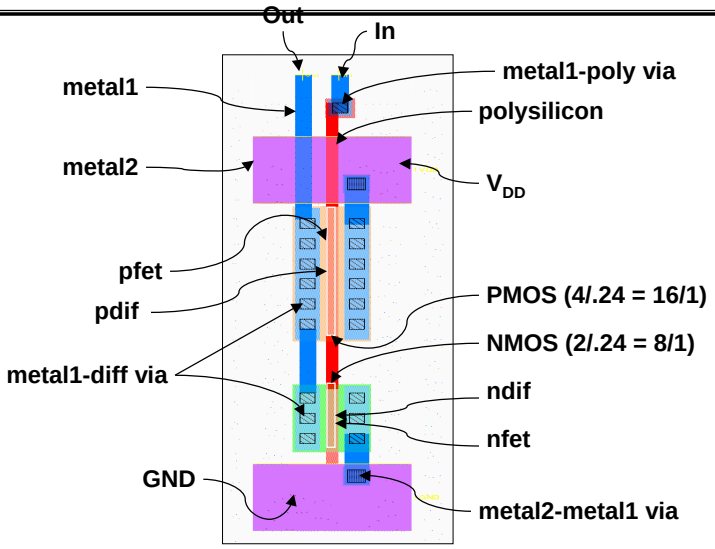


max Layer Representation



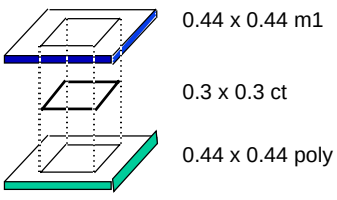
- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support “stacked vias”
- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))
- Wells (nw) and other select areas (pplus, nplus, prb)

CMOS Inverter *max* Layout

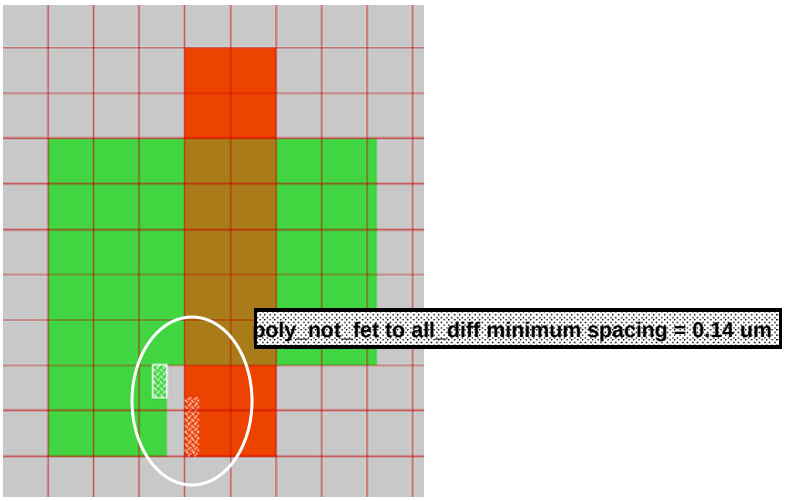


Simplified Layouts in *max*

- Online design rule checking (DRC)
- Automatic fet generation (just overlap poly and diffusion and it creates a transistor)
- Simplified via/contact generation
  - v12, v23, v34, v45
  - ct, nwc, pwc



Design Rule Checker



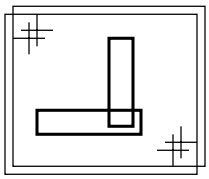
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

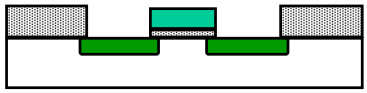
To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

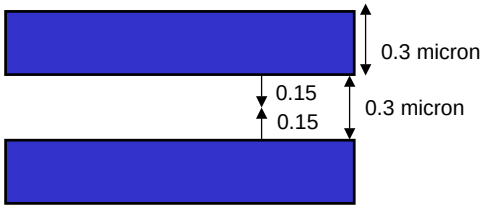
3. Process parameters (e.g., lateral diffusion)



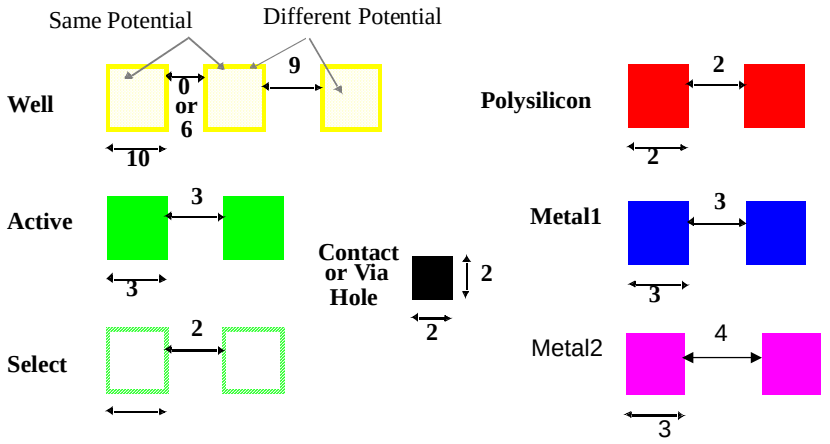
4. Rough surfaces

Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab

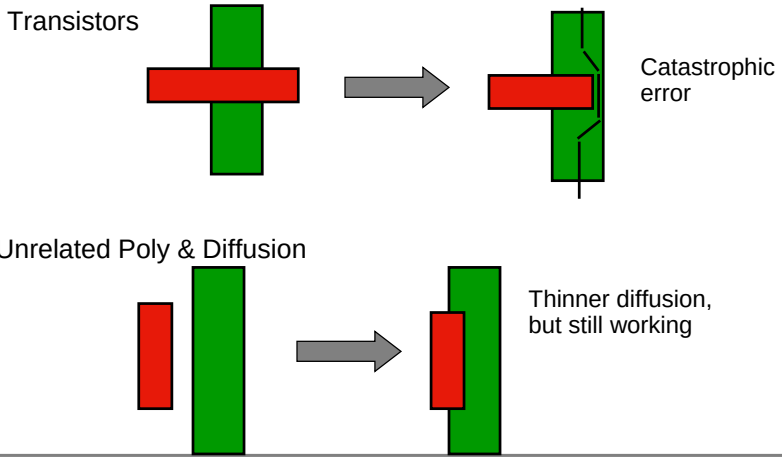


Intra-Layer Design Rules

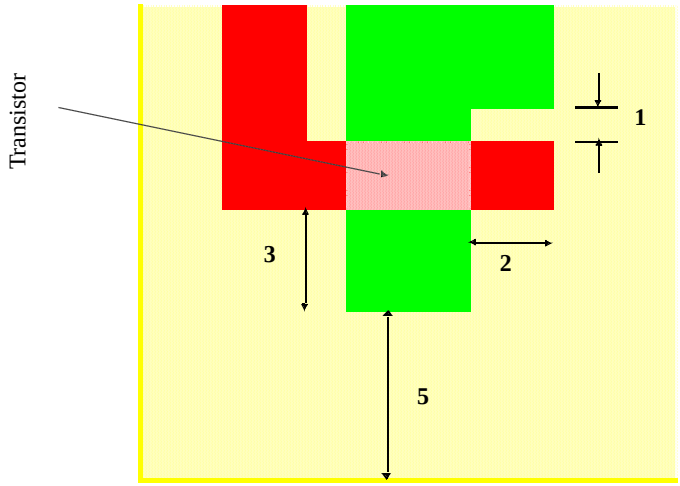


Inter-Layer Design Rule Origins

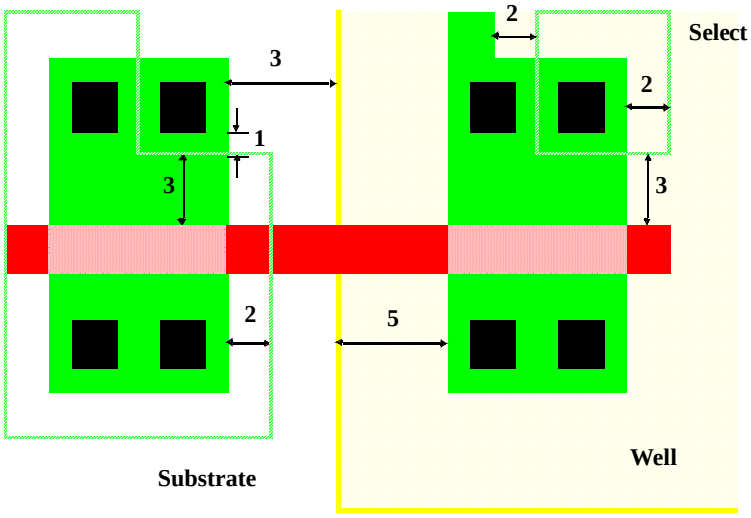
1. Transistor rules – transistor formed by overlap of active and poly layers



Transistor Layout

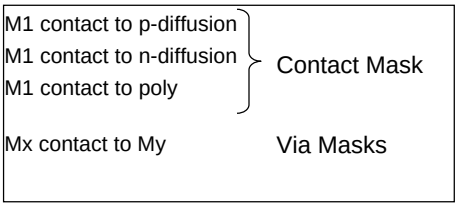


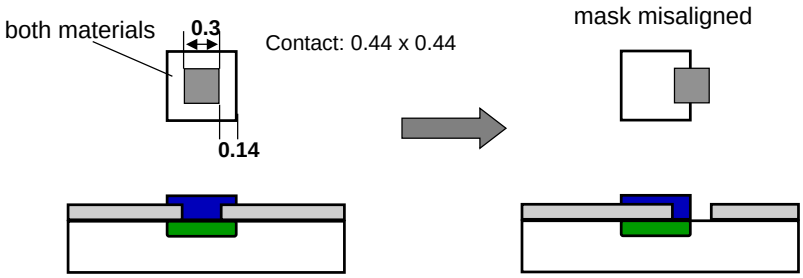
Select Layer



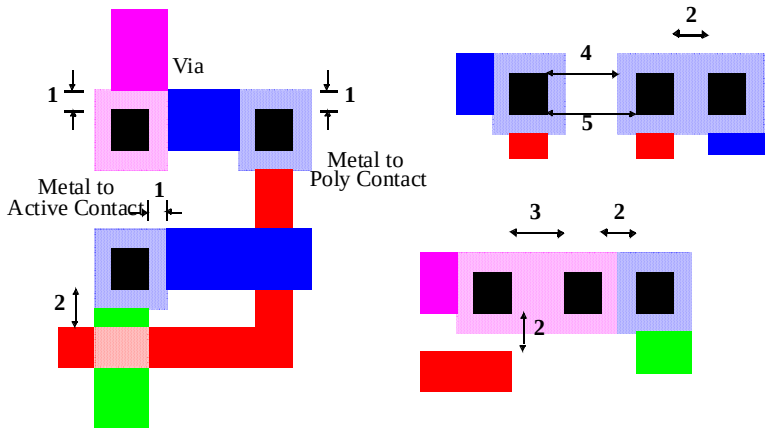
Inter-Layer Design Rule Origins, Con't

2. Contact and via rules





Vias and Contacts



CMOS Process Layers

Mask/Layer name	Derivation from drawn layers	Alternative names for mask/layer	MOSIS mask label
n-well	=nwell	bulk, substrate, tub, n-tub, moat	CWN
p-well	=pwell	bulk, substrate, tub, p-tub, moat	CWP
active	=pdiff+ndiff	thin oxide, thinox, island, gate oxide	CAA
polysilicon	=poly	poly, gate	CPG
n-diffusion implant	=grow(ndiff)	ndiff, n-select, nplus, n+	CSN
p-diffusion implant	=grow(pdiff)	pdiff, p-select, pplus, p+	CSP
contact	=contact	contact cut, poly contact, diffusion contact	CCP and CCA
metal1	=m1	first-level metal	CMF
metal2	=m2	second-level metal	CMS
via2	=via2	metal2/metal3 via	CVS
metal3	=m3	third-level metal	CMT
glass	=glass	passivation, overglass, pad	COG

Summary

- MOS Transistors are stack of gate, oxide, silicon
- Can be viewed as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Now you know everything necessary to start designing schematics and layout for a simple chip!

To probe further

- http://www.leb.e-technik.uni-erlangen.de/lehre/mm/html/start.htm