CPE/EE 427, CPE 527
VLSI Design I
L06: Complementary CMOS Logic Gates

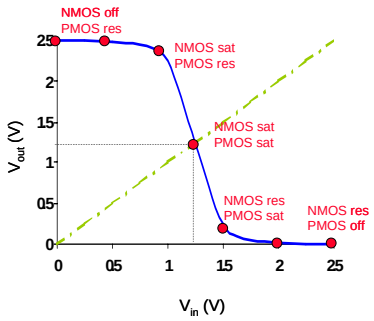
Department of Electrical and Computer Engineering
University of Alabama in Huntsville

Aleksandar Milenkovic (www.ece.uah.edu/~milenka)
www.ece.uah.edu/~milenka/cpe527-05F

Course Administration

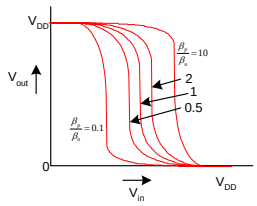
- Instructor: Aleksandar Milenkovic
  milenka@ece.uah.edu
  www.ece.uah.edu/~milenka
  EB 217-L
  Mon. 5:30 PM – 6:30 PM,
  Wen. 12:30 – 13:30 PM
- URL: http://www.ece.uah.edu/~milenka/cpe527-05F
- TA: Joel Wilder
- Labs: Lab#2 posted (due 9/23/05)
- Text: CMOS VLSI Design, 3rd ed., Weste, Harris
- Review: Introduction, Design Metrics, IC Fabrication (Read Chapter 1); IC Fabrication (Chapter 3)
- Today: MOS Non-ideal IV, CMOS Inverter (Chapter 2)

CMOS Inverter VTC



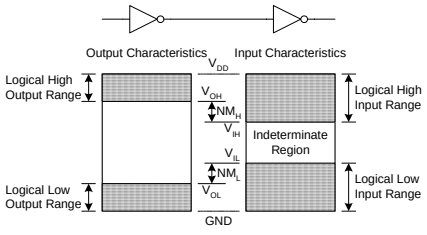
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



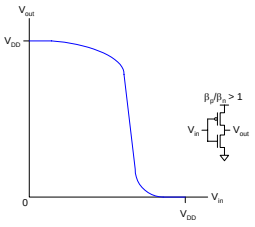
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



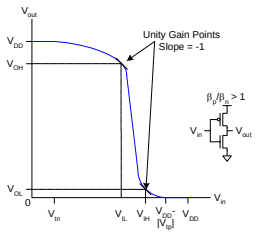
Logic Levels

- To maximize noise margins, select logic levels at

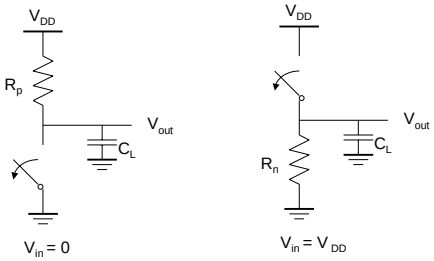


Logic Levels

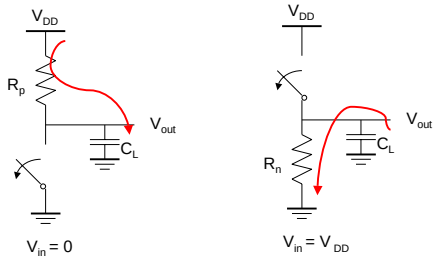
- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



CMOS Inverter: Switch Model of Dynamic Behavior



CMOS Inverter: Switch Model of Dynamic Behavior



Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

Switching Threshold

- V_M where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)

  $V_M \approx rV_{DD}/(1 + r)$ where $r = k_pV_{DSATp}/k_nV_{DSATn}$
- Switching threshold set by the ratio r, which compares the relative driving strengths of the PMOS and NMOS transistors
- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n'V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k_p'V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)}$$

Switch Threshold Example

- In our generic 0.25 micron CMOS process, using the process parameters from slide L03.25, a $V_{DD} = 2.5V$, and a minimum size NMOS device ($(W/L)_n$ of 1.5)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2)	λ(V^{-1})
NMOS	0.43	0.4	0.63	115 x 10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30 x 10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} =$$

Switch Threshold Example

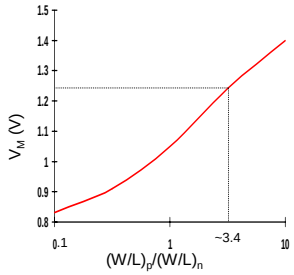
- In our generic 0.25 micron CMOS process, using the process parameters, a V_{DD} = 2.5V, and a minimum size NMOS device ($(W/L)_n$ of 1.5)

	V_{T0}(V)	$\gamma(V^{0.5})$	V_{DSAT}(V)	k'(A/V^2)	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115 x 10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30 x 10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

$(W/L)_p$ = 3.5 x 1.5 = 5.25 for a V_M of 1.25V

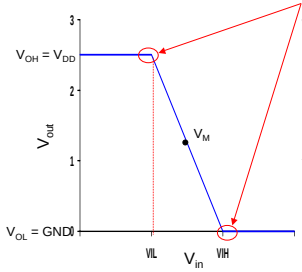
Simulated Inverter V_M



Note: x-axis is semilog

- V_M is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives V_M's of 1.22V, 1.18V, and 1.13V
- Increasing the width of the PMOS moves V_M towards V_{DD}
- Increasing the width of the NMOS moves V_M toward GND

Noise Margins Determining V_{IH} and V_{IL}



A piece-wise linear approximation of VTC

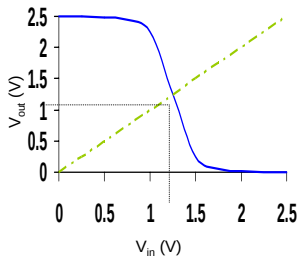
By definition, V_{IH} and V_{IL} are where dV_{out}/dV_{in} = -1 (= gain)

$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL} - GND$

Approximating:
$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

So high gain in the transition region is very desirable

CMOS Inverter VTC from Simulation



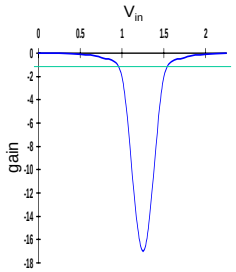
0.25um, $(W/L)_p/(W/L)_n$ = 3.4
$(W/L)_n$ = 1.5 (min size)
V_{DD} = 2.5V

$V_M \approx$ 1.25V, g = -27.5

V_{IL} = 1.2V, V_{IH} = 1.3V
$NM_L = NM_H$ = 1.2
(actual values are
V_{IL} = 1.03V, V_{IH} = 1.45V
NM_L = 1.03V & NM_H = 1.05V)

Output resistance
low-output = 2.4kΩ
high-output = 3.3kΩ

Gain Determinates

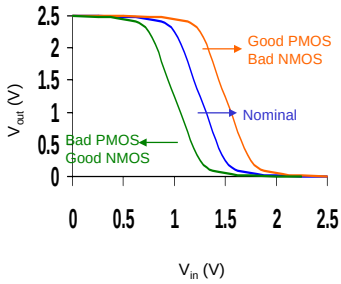


Gain is a strong function of the slopes of the currents in the saturation region, for $V_{in} = V_M$

$$g \approx \frac{(1+r)}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

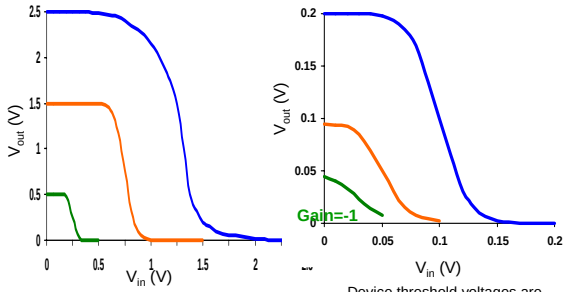
Determined by technology parameters, especially channel length modulation (λ). Only designer influence through supply voltage and V_M (transistor sizing).

Impact of Process Variation on VTC Curve



process variations (mostly) cause a shift in the switching threshold

Scaling the Supply Voltage



Device threshold voltages are kept (virtually) constant

Device threshold voltages are kept (virtually) constant

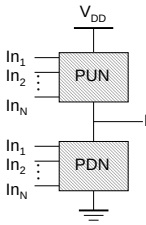
Static CMOS Logic

CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - VOH and VOL are at VDD and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between VDD and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)
- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

Static Complementary CMOS

Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

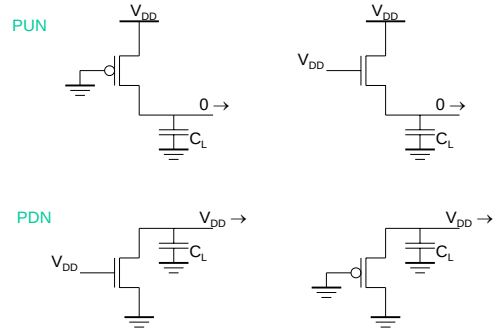
pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,...In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,...In_N) = 0$

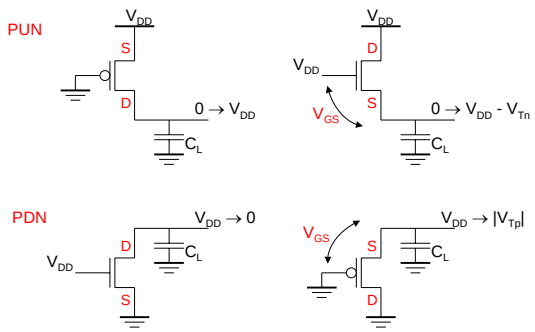
NMOS transistors only

PUN and PDN are dual logic networks

Threshold Drops

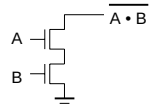


Threshold Drops

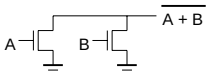


Construction of PDN

- NMOS devices in series implement a NAND function



- NMOS devices in parallel implement a NOR function



Dual PUN and PDN

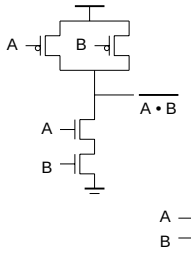
- PUN and PDN are dual networks
  - DeMorgan's theorems

$\overline{A + B} = \overline{A} \cdot \overline{B}$ [!(A + B) = !A • !B or !(A | B) = !A & !B]

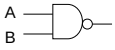
$\overline{A \cdot B} = \overline{A} + \overline{B}$ [!(A • B) = !A + !B or !(A & B) = !A | !B]

  - a parallel connection of transistors in the PUN corresponds to a series connection of the PDN
- Complementary gate is naturally inverting (NAND, NOR, AOI, OAI)
- Number of transistors for an N-input logic gate is 2N

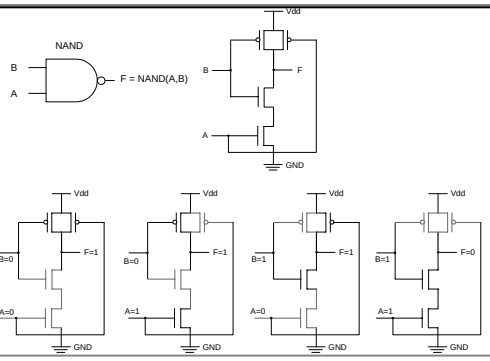
CMOS NAND



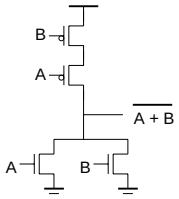
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



CMOS NAND

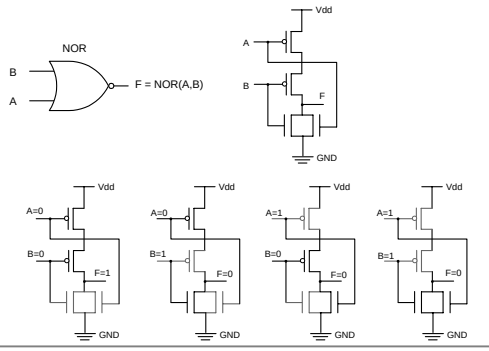


CMOS NOR

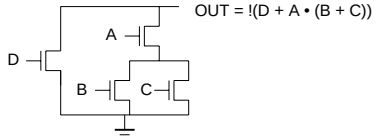


A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

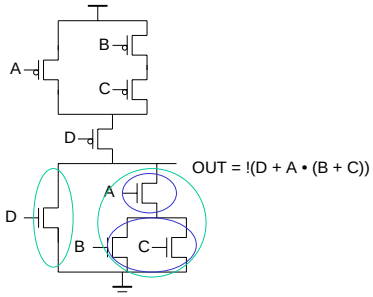
CMOS NOR



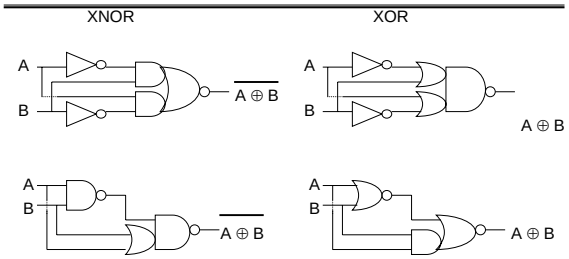
Complex CMOS Gate



Complex CMOS Gate



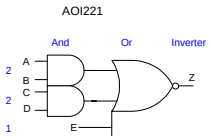
XNOR/XOR Implementation



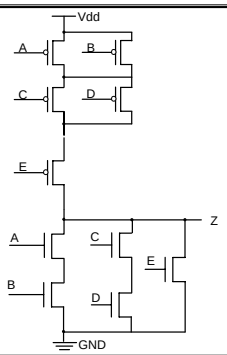
- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?

Combinational Logic Cells

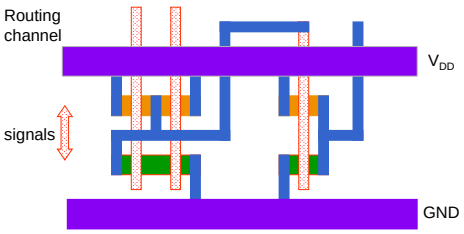
- CMOS logic cells
  - AND-OR-INVERT (AOI)
  - OR-AND-INVERT(OAI)
- Example: AOI221
  Z = (A*B + C*D + E)'
  Z = AOI221(A, B, C, D, E)
  Exercise: Construct this logic cell?
- Example: OAI321
  Z = [(A+B+C)*(D+E)*F]'
  Z = OAI321(A, B, C, D, E, F)
  Exercise: Construct this logic cell?



AOI221

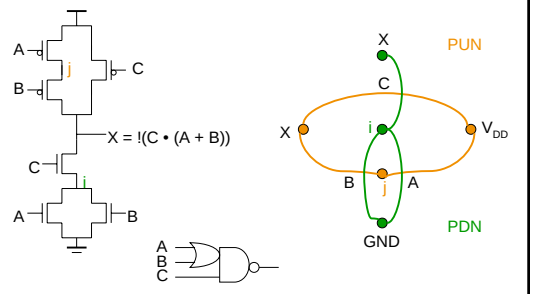


Standard Cell Layout Methodology

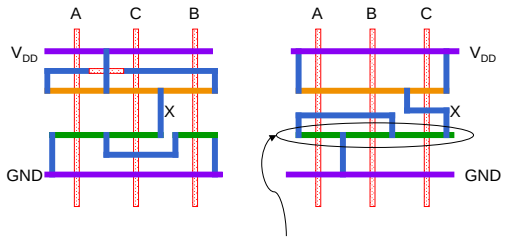


What logic function is this?

OAI21 Logic Graph

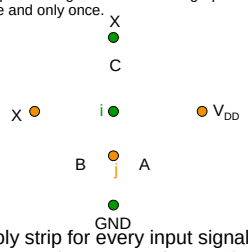


Two Stick Layouts of !(C • (A + B))



Consistent Euler Path

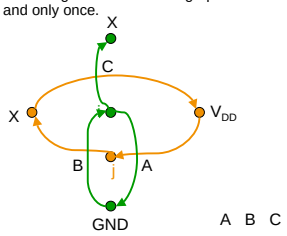
- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.



- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

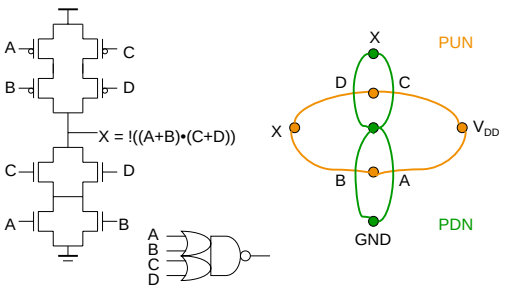
Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

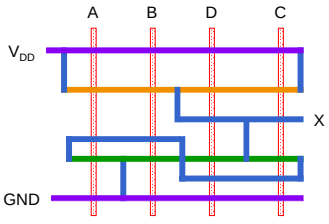


- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

OAI22 Logic Graph



OAI22 Layout



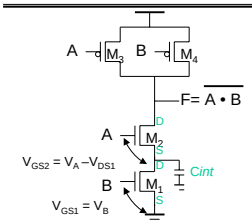
- Some functions have no consistent Euler path like x = !(a + bc + de) (but x = !(bc + a + de) does!)

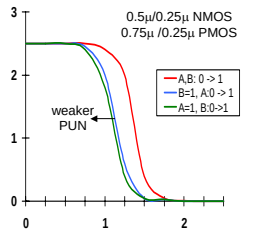
Combinational Logic Cells (cont'd)

- The AOI family of cells with 3 index numbers or less
  - X = {AOI, OAI, AO, OA}; a,b,c={2,3}

Cell Type	Cells	Number of Unique Cells
Xa1	X21, X31	2
Xa11	X211, X311	2
Xab	X22, X33, X32	3
Xab1	X221, X321, X331	3
Xabc	X222, X333, X332, X322	4
Total		**14**

VTC is Data-Dependent





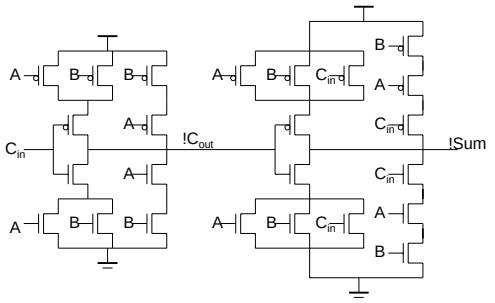
- The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

$V_{Tn1} = V_{Tn0}$

$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{(|2\phi_F| + V_{int})} - \sqrt{|2\phi_F|})$

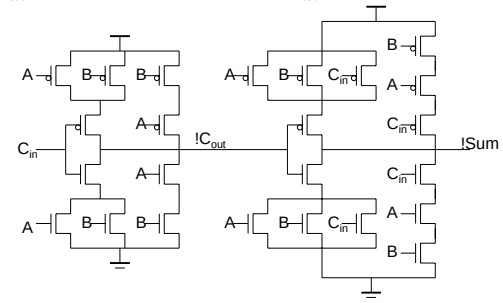
since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of *Cint*

Static CMOS Full Adder Circuit



Static CMOS Full Adder Circuit

$!C_{out} = !C_{in}$ & (!A | !B) | (!A & !B) $!Sum = C_{out}$ & (!A | !B | $!C_{in}$) | (!A & !B & $!C_{in}$)



$C_{out} = C_{in}$ & (A | B) | (A & B) Sum = $!C_{out}$ & (A | B | C_{in}) | (A & B & C_{in})