Syllabus: CPE 626 -
Advanced VLSI Design, Fall 2004

Instructor: Dr. Aleksandar Milenkovic — Email: milenka@ece.uah.edu
Office: 217-L — Phone: (256) 824 6830

Time and Place: Lectures: MW 5:30 – 6:50 PM, Engineering Building 229

Course Web Page: www.ece.uah.edu/~milenka/cpe626-04F/

Office Hours: MW 7:00-8:00 PM or by appointment.

Reference Texts:

a. J. Rabaey, A. Chandarakasan, B. Nikolic, Digital Integrated Circuits: A Design Perspective Prentice Hall, 2/e, ISBN 0-13-090996-3.

b. Michael John Sebastian Smith, Application-Specific Integrated Circuits, Addison-Wesley, 1997. ISBN: 0201500221. http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/ASICs.htm

c. Peter J. Ashenden, *The Designer's Guide to VHDL (2nd edition)*, Morgan-Kaufmann Publishers, 2002 (ISBN: 1-55860-674-2).

d. K. C. Chang, *Digital Systems Design with VHDL and Synthesis - An Integrated Approach*, IEEE Computer Society, 1999.

Prerequisites: CPE 526

Course Description:

In the future we will need more customized, application-specific solutions, which can provide the performance needed at a lower cost than general-purpose architectures. Because cost and time-to-market constraints are very important to such systems, architecture should permit automatic design, including high-level architectural design.

In this course we will present a new design methodology based on using modern hardware description languages such as VHDL, Verilog, and SystemC. The course addresses algorithm, architecture, and implementation aspects of common building blocks (arithmetic processing elements, filters, processor cores, etc). .

Topics:

- Languages for VLSI synthesis: VHDL, Verilog, SystemC.
- FPGA hardware structures.
- Design and analysis of algorithm-specific VLSI processor architectures. Topics include the implementation of pipelined and systolic processor structure. Techniques for mapping numerical algorithms onto custom processor arrays, including Application Specific Instruction Processors (ASIPs).
- Prototyping using Xilinx ISE and Xilinx FPGAs.
- High-level DSP algorithm simulation and code generation.

Grading Policy:

1. Homeworks	20%
2. Midterm Exam	25%
3. Essay	15%
4. Project	35%
5. Class participation	5%

Homeworks must be submitted at the beginning of class on the day they are due. Homework submitted more than one week late will not be graded. Late homeworks will be penalized 30% for the first day late, and 10% per day thereafter. All requests for a re-grade must be submitted in writing within a week of the assignment being returned. No assignment will be re-graded after one week. Please let me know immediately if I have added up your score incorrectly.

Grades will be determined on a 60-70-80-90 straight scale. On occasion I may use a slightly lower scale, but I will never raise the requirements.

Tentative Schedule of Important Class Dates

1. October 4	Project proposals due
2. October 20	Midterm Exam
3. November 15	Essay due
4. December 6/8	Project presentations5. December 13 Project and final report due

I reserve the right to change the above schedule based upon the needs of the course.

Academic Honesty: Discussing the homework with other students is encouraged, as that is one of the best ways to learn the material. But the work submitted should be your own. All students will be trusted to pursue their academic careers with honesty and integrity. Academic dishonesty includes, but not limited to, cheating on a test or other course work, plagiarism, unauthorized collaboration with other persons. Students found guilty of dishonesty will be subject to penalties that may include suspension from the university.