1. program counter
2. data path
3. target address
4. tristate buffer
5. Abstract
6. (5 points) The PowerPC 601 processor addresses a maximum of 2^{48} bytes of memory. What is the maximum number of 32-bit words that can be stored in this memory?

$$2^{48} bytes \times \frac{1 word}{32 bits} \times \frac{8 bits}{1 byte} = 2^{46} words$$

7. (10 points) Represent 227 and -326 as signed 16-bit numbers

```
                          2    0   1
2    0   1                2    1   0
2    1   1                2    2   1
2    3   1                2    5   0
2    7   0                2   10   0
2   14   0                2   20   0
2   28   0                2   40   1
2   56   1                2   81   1
2  113   1                2  163   0
2  227                    2  326
```

```
227 = 0000 0000 1110 0011
326 =  0000 0001 0100 0110
-326 = 1111 1110 1011 1010
```

8.

	Initial Value	Second Value	Third Value	Fourth Value	Fifth Value	Sixth Value	Seventh Value
r0		-2	-1	0			
r1	0	1	2	3			
r2	8020						
r3	0	4	8	12			
r4	0						
r5	1	2	3	4			

Results of the `st` instruction.

Memory Address	Contents
0	1
4	2
8	3

9.

```
          cnt:   .equ 8
                  .org 0
0x0000    seq:   .dc 1
0x0004    next:  .dc 1
0x0008    ans:   .dw cnt
                  .org 0x1000
0x1000           lar   r31, loop
0x1004           la    r0, cnt
0x1008           la    r1, seq
0x100C    loop:  ld    r2, 0(r1)
0x1010           ld    r3, 4(r1)
0x1014           add   r2, r2, r3
0x1018           st    r2, 8(r1)
0x101C           addi  r1, r1, 4
0x1020           addi  r0, r0, -1
0x1024           brnz  r31, r0
```

Address	Label	Instruction	op	ra	rb	rc	c1	c2	c3	Hexadecimal
0x1000		lar 31, loop	6	31	-	-	8	-	-	37C0 0008
0x1014		add r2, t2, r3	12	2	2	3	-	-	-	6084 3000
0x1024		brnz r31, r0	8	-	31	0	-	-	3	403E 0003

10. (25 points) Write the code to implement the expression A = (B + C)*D) – (E/F) on 3-, 2-, 1-, and 0-address machines. Do not rearrange the expression. In accordance with programming language practice, computing the expression should not change the values of its operands.

3-address

```
add   A, B, C
mpy   A, A, D
div   T, E, F
sub   A, A, T
```

2-address

```
load   A, B
add    A, C
mpy    A, D
load   T, E
div    T, F
sub    A, T
```

1-address

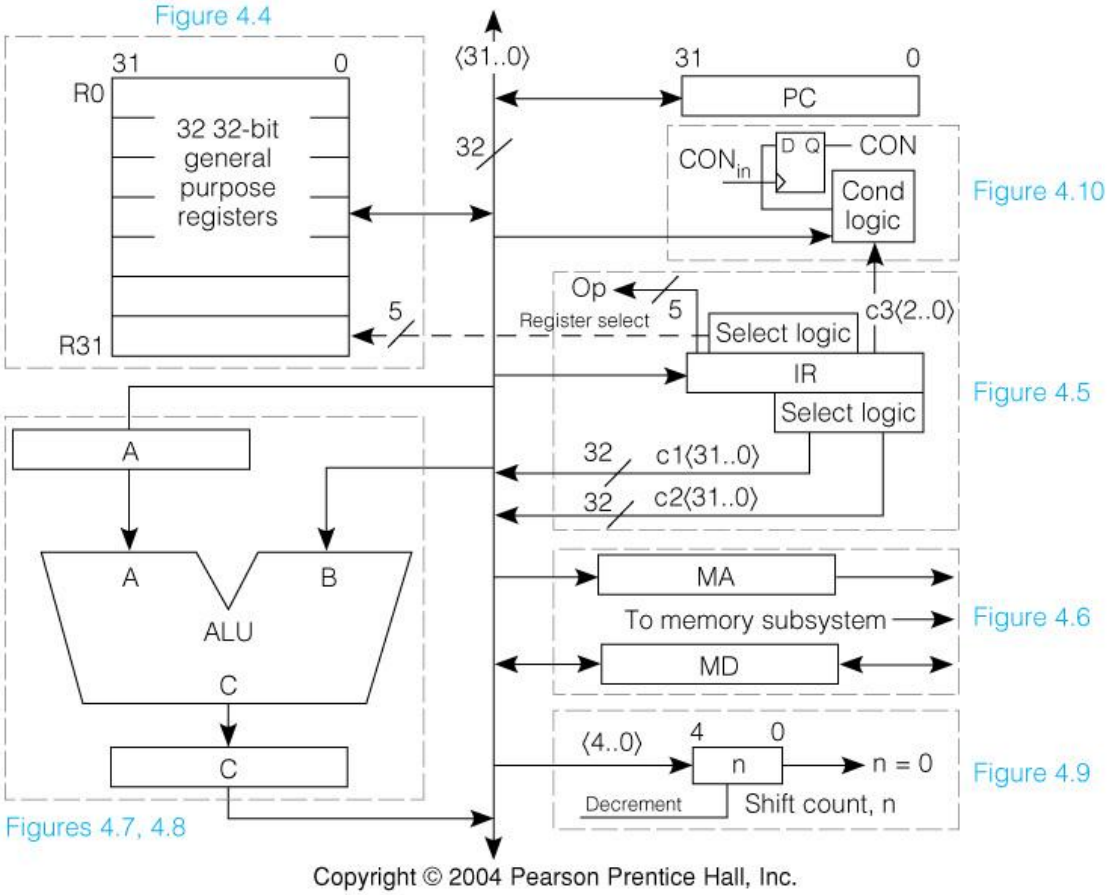
```
load   E
sub    F
store  T
load   B
```

```
add     C
mpy     D
sub     T
store   A
```

0-address

```
push    B
push    C
add
push    D
mpy
push    E
push    F
div
sub
pop     A
```

11. (20 points) Write concrete RTN steps for the SRC instruction ldr using the 1-bus SRC microarchitecture shown.



T0	MA ← PC: C ← PC + 4;
T1	PC ← C: MD ← M[MA];
T2	IR ← MD;
T3	A ← PC;
T4	C ← A + c1 {sign extend};
T5	R[ra] ← C
T6	
T7	