The University of Alabama in Huntsville
Electrical and Computer Engineering Department
CPE 221 01
Fall 2012
Sample Test 2

1. (1 point).Pipelining is a technique for improving the _____ of instruction execution.
2. (1 point) In _____ microcode, each control signal is represented by a bit in the microinstruction.
3. (1 point) In _____ microcode, each distinct microinstruction is encoded as a single signal that is fanned out to the control signals that are to be asserted.
4. (1 point) _____ RAM requires refreshing.
5. (1 point) The bit line _____ operation that causes the difference between access time and cycle time

6. (6 points) r2 contains a value of 6 in decimal. What is the decimal value of r1 after these instructions are executed? The instructions are independent of each other. (6 points)

   (a) shr r1, r2, 2

   (b) shl r1, r2, 2

7. (2 points) Which memory is the smallest? Select one.

   (a) register (b) cache memory (c) main memory (d) disk memory

8-12. (15 points) What are the values of the following registers and memory address when the program executes "`brzr r29, r4`" for the first time? Answer in decimal.

8. r3: _____ 9. r2: _____

10. r5: _____ 11. r4: _____

12. r1: _____

```
            .org   200
count:      .dw   1
bits:       .dw   1
num:        .dc   65226
mask:       .dc   1

orig:       .org  1000
            lar   r30, done
            lar   r29, shift
            lar   r28, next
            ld    r1, num
            ld    r3, mask
            brzr  r30, r1
            sub   r2, r2, r2
            sub   r5, r5, r5
next:       and   r4, r1, r3
            addi  r5, r5, 1
            brzr  r29, r4
            addi  r2, r2, 1
shift:      shr   r1, r1, 1
            brnz  r28, r1
done:       st    r2, count
            st    r5, bits
            stop
```

13. (2 points) Which is **not** a register in SRC?
    a. 32 general purpose registers b. a program counter
    c. a status register d. an instruction register

14. (2 points)Which is the **incorrect** statement on the following branch instruction?
    brl ra, rb, rc, c3
    a. It checks whether R[rc] meets conditions in c3.
    b. If the condition is true, it branches to R[rb].
    c. If the condition is true, it copies PC to R[ra].
    d. *ra* is the link register allowing return from subroutine calls.

15. (2 points) These are the RTN descriptions on effective address calculations on two addressing modes.

    disp<31..0> := ((rb = 0) $\rightarrow$ c2<16..0> {sign extend}: Displacement
    (rb $\neq$ 0) $\rightarrow$ R[rb] + c2<16..0> {sign extend, 2's complement}):
    rel<31..0> := PC<31..0> + c1<21..0> {sign extend, 2's complement}: Relative

    a. Both displacement and relative addressing mode are correct.
    b. Neither displacement nor relative addressing mode are correct.
    c. Displacement addressing mode is correct, but relative addressing mode is incorrect.
    d. Displacement addressing mode is incorrect, but relative addressing mode is correct.

16. (2 points) Suppose that R[rc] contains 80000000H. When does a branch not occur?
    a. c3<2..0> = 1
    b. c3<2..0> = 3
    c. c3<2..0> = 4
    d. c3<2..0> = 5

17. (2 points)This is 1-bus microarchitecture. We add new registers not found in the abstract RTN. Which is incorrect?
    a. A, B, and C registers are needed to temporarily store two operands and the result when doing ALU operations.
    b. MA and MD registers are used as interface registers to the memory system.
    c. MA contains the address of the memory operand.
    d. MD is used as a buffer for outgoing and incoming values.
    e. None of the above

18. (2 points)Which is incorrect in 1-bus SRC?
    a. MA only receives data from the bus and passes it on to the memory subsystem.
    b. MD is unidirectional: it sends data to the memory subsystem upon a "write" and receives data from the memory system upon a "read."
    c. The 5-bit register, n, stores the shift count, and in this design n is a counter that can be decremented.
    d. The Cond logic employs the least significant 3 bits of the c3 field in the IR, which specify the condition to be tested in conditional branch instruction, as well as the bus contents to compute whether a given condition is true.
    e. None of the above

19. (2 points) If the maximum clock frequency is 1250 MHz and we assume no safety margin, what is the minimum clock period?
    a. 1.6 ns b. 800 ps c. 1.6 ps d. 800 ns

20. (2 points)Which is the incorrect statement in 2-bus SRC?
    a. It has two buses, "In bus" and "Out bus".
    b. It can eliminate *A* register.
    c. The ALU function C = B copies the contents of the B bus to the C output of the ALU, and from there to the A bus.
    d. Performance is improved due to the decrease in the average number of clock cycles required to execute a given program, but it may be offset by an increase in the minimum clock period.
    e. None of the above

21. (2 points)Which is the incorrect assumption in pipeline design?
    a. The instruction set is unchanged.
    b. Two separate memories are needed, one for program and the other for data.
    c. Virtually all pipelined designs require a 2-port register file to allow the reading of one operand and the writing of the other in a single clock cycle.
    d. Pipelined designs replace the buses with direct connections between registers.

22. (2 points) Which is incorrect explaining the global state of the pipelined SRC?
    a. Instruction memory is only accessed in Stage 1.
    b. PC is only accessed in Stage 1.
    c. General registers are read in Stage 2 and written in Stage 5.
    d. Data memory is only accessed in Stage 4.

23. (2 points) There are 16 ALU and 5 branch control signals. If we use a 4-16 decoder and a 3-8 decoder in vertical microcode, how many bits are saved compared to horizontal microcode?
a. 16 b. 8 c. 7 d. 14

24. (10 points) Design a microcode sequence to implement the 1-bus SRC *ld* instruction using the concrete RTN of Table 4.9 and 4.6. Refer to Table 5.2 and 5.3.

address	100	101	102	600	601	602	603	604
Mux control								
PC_{out}								
C_{out}								
MD_{out}								
R_{out}								
$c2_{out}$								
BA_{out}								
MA_{in}								
C_{in}								
A_{in}								
R_{in}								
PC_{in}								
IR_{in}								
ADD								
INC4								
Wait								
Read								
Write								
Wait								
Gra								
Grb								
Grc								
End								

28. (30 points) Write an SRC assembly language program to implement the following C statements, assuming all variables are 32-bit integers.

```
n = 10;
sum = 0;
for (i = 0; i < n; i++)
   sum = sum + i;
```

29. (10 points) Identify all of the data dependencies in the following code.

```
add   r2, r5, r4
ld    r4, 28(r2)
add   r5, r4, r5
st    r5, 100(r2)
add   r6, r5, r8
brpl  r29, r4
```