

The University of Alabama in Huntsville
Electrical and Computer Engineering Department
CPE 221 01
Fall 2012
Sample Test 2 Solution

1. (1 point).Pipelining is a technique for improving the throughput of instruction execution.
2. (1 point) In horizontal microcode, each control signal is represented by a bit in the microinstruction.
3. (1 point) In vertical microcode, each distinct microinstruction is encoded as a single signal that is fanned out to the control signals that are to be asserted.
4. (1 point) Dynamic RAM requires refreshing.
5. (1 point) The bit line precharge operation that causes the difference between access time and cycle time

6. (6 points) r2 contains a value of 6 in decimal. What is the decimal value of r1 after these instructions are executed? The instructions are independent of each other. (6 points)
 - (a) shr r1, r2, 2
1
 - (b) shl r1, r2, 2
24

7. (2 points) Which memory is the smallest? Select one. **A**
 - (a) register
 - (b) cache memory
 - (c) main memory
 - (d) disk memory

8-12. (15 points) What are the values of the following registers and memory address when the program executes “brzr r29, r4” for the first time? Answer in decimal.

8. r3: 1 9. r2: 0
10. r5: 1 11. r4: 0
12. r1: 65226

```

count:      .org    200
            .dw    1
bits:       .dw    1
num:        .dc    65226
mask:       .dc    1

orig:       .org    1000
            lar    r30, done
            lar    r29, shift
            lar    r28, next
            ld     r1, num
            ld     r3, mask
            brzr   r30, r1
            sub    r2, r2, r2
            sub    r5, r5, r5
next:       and    r4, r1, r3
            addi   r5, r5, 1
            brzr   r29, r4
            addi   r2, r2, 1
shift:     shr    r1, r1, 1
            brnz   r28, r1
done:      st     r2, count
            st     r5, bits
            stop

```

13. (2 points) Which is **not** a register in SRC? **C**
- 32 general purpose registers
 - a program counter
 - a status register**
 - an instruction register
14. (2 points) Which is the **incorrect** statement on the following branch instruction? **All of these are correct, however, c does not mention a branch, this question will not be on your test.**
- brl ra, rb, rc, c3**
- It checks whether R[rc] meets conditions in c3.
 - If the condition is true, it branches to R[rb].
 - If the condition is true, it copies PC to R[ra].**
 - ra is the link register allowing return from subroutine calls.
15. (2 points) These are the RTN descriptions on effective address calculations on two addressing modes. **A**

$\text{disp}\langle 31..0 \rangle := ((rb = 0) \rightarrow c2\langle 16..0 \rangle \{\text{sign extend}\}):$ Displacement
 $(rb \neq 0) \rightarrow R[rb] + c2\langle 16..0 \rangle \{\text{sign extend, 2's complement}\}):$
 $\text{rel}\langle 31..0 \rangle := PC\langle 31..0 \rangle + c1\langle 21..0 \rangle \{\text{sign extend, 2's complement}\}):$ Relative

- Both displacement and relative addressing mode are correct.**
- Neither displacement nor relative addressing mode are correct.
- Displacement addressing mode is correct, but relative addressing mode is incorrect.
- Displacement addressing mode is incorrect, but relative addressing mode is correct.

16. (2 points) Suppose that R[rc] contains 80000000H. When does a branch not occur? **C**
- $c3<2..0> = 1$
 - $c3<2..0> = 3$
 - $c3<2..0> = 4$**
 - $c3<2..0> = 5$
17. (2 points) This is 1-bus microarchitecture. We add new registers not found in the abstract RTN. Which is incorrect? **A**
- A, B, and C registers are needed to temporarily store two operands and the result when doing ALU operations.**
 - MA and MD registers are used as interface registers to the memory system.
 - MA contains the address of the memory operand.
 - MD is used as a buffer for outgoing and incoming values.
 - None of the above
18. (2 points) Which is incorrect in 1-bus SRC? **B**
- MA only receives data from the bus and passes it on to the memory subsystem.
 - MD is unidirectional: it sends data to the memory subsystem upon a "write" and receives data from the memory system upon a "read."**
 - The 5-bit register, n, stores the shift count, and in this design n is a counter that can be decremented.
 - The Cond logic employs the least significant 3 bits of the c3 field in the IR, which specify the condition to be tested in conditional branch instruction, as well as the bus contents to compute whether a given condition is true.
 - None of the above
19. (2 points) If the maximum clock frequency is 1250 MHz and we assume no safety margin, what is the minimum clock period? **B**
- 1.6 ns
 - 800 ps**
 - 1.6 ps
 - 800 ns
20. (2 points) Which is the incorrect statement in 2-bus SRC? **B**
- It has two buses, "In bus" and "Out bus".
 - It can eliminate A register.**
 - The ALU function $C = B$ copies the contents of the B bus to the C output of the ALU, and from there to the A bus.
 - Performance is improved due to the decrease in the average number of clock cycles required to execute a given program, but it may be offset by an increase in the minimum clock period.
 - None of the above
21. (2 points) Which is the incorrect assumption in pipeline design? **C**
- The instruction set is unchanged.
 - Two separate memories are needed, one for program and the other for data.
 - Virtually all pipelined designs require a 2-port register file to allow the reading of one operand and the writing of the other in a single clock cycle.**
 - Pipelined designs replace the buses with direct connections between registers.
22. (2 points) Which is incorrect explaining the global state of the pipelined SRC? **B**
- Instruction memory is only accessed in Stage 1.
 - PC is only accessed in Stage 1.**
 - General registers are read in Stage 2 and written in Stage 5.
 - Data memory is only accessed in Stage 4.

28. (30 points) Write an SRC assembly language program to implement the following C statements, assuming all variables are 32-bit integers.

```
n = 10;
sum = 0;
for (i = 0; i < n; i++)
    sum = sum + i;
```

```
.org 100
n:   .dc 10
sum: .dw 1
     .org 2000
     lar  r30, done
     lar  r29, loop
     ld   r2, n
     sub  r1, r1, r1
     sub  r3, r3, r3
loop: sub  r4, r1, r2
     brpl r30, r4
     add  r3, r3, r1
     addi r1, r1, 1
     br   r29
done: st   r3, sum
     stop
```

29. (10 points) Identify all of the data dependencies in the following code.

- a. add r2, r5, r4
- b. ld r4, 28(r2)
- c. add r5, r4, r5
- d. st r5, 100(r2)
- e. add r6, r5, r8
- f. brpl r29, r4

Instruction a produces a value of r2 that is needed by instruction b and instruction d
Instruction b produces a value of r4 that is needed by instruction c and by instruction f
Instruction c produces a value of r5 that is needed by instruction d and instruction e