

The University of Alabama in Huntsville
Electrical and Computer Engineering Department
CPE 221 01
Fall 2012
Test 1 Solution

1. (1 point) The **_program counter_** contains information about the location of the next instruction.
2. (1 point) The design of the storage cells and the interconnections between them is known as the **_data path_**.
3. (1 point) A **_target address_** is the address to which control is transferred as a result of a branch instruction.
4. (1 point) A **_tristate buffer_** is used to control what is allowed to drive a bus.
5. (1 point) **_Abstract_** RTN is implementation independent.
6. (5 points) The PowerPC 601 processor addresses a maximum of 2^{48} bytes of memory. What is the maximum number of 32-bit words that can be stored in this memory?

$$2^{48} \text{ bytes} \times \frac{1 \text{ word}}{32 \text{ bits}} \times \frac{8 \text{ bits}}{1 \text{ byte}} = 2^{46} \text{ words}$$

7. (10 points) Represent 154 and -199 as signed 16-bit numbers

2	0	1	2	0	1
2	1	0	2	1	1
2	2	0	2	3	0
2	4	1	2	6	0
2	9	1	2	12	0
2	19	0	2	24	1
2	38	1	2	49	1
2	77	0	2	99	1
2	154		2	199	

154 = 0000 0000 1001 1010
 199 = 0000 0000 1100 0111
 -199 = 1111 1111 0011 1001

8. (20 points) Consider the following SRC program. Trace the values of the registers shown as they change during program execution. Also, trace the writes to memory by the st instruction. There may be unused columns or rows in the tables. If you need to add columns or rows, you may do so.

```

cnt:  .equ 5
      .org 0
seq:  .dc 1
next: .dc 1
ans:  .dw cnt
      .org 0x1000
      lar r31, loop
      la  r0, cnt
      la  r1, seq
loop: ld  r2, 0(r1)
      ld  r3, 4(r1)
      add r2, r2, r3
      st  r2, 8(r1)
      addi r1, r1, 4
      addi r0, r0, -1
      brnz r31, r0

```

	Initial Value	Second Value	Third Value	Fourth Value	Fifth Value	Sixth Value	Seventh Value	Eighth Value	Ninth Value	Tenth Value
r0	5	4		3		2		1		0
r1	0	4		8		12		16		20
r2	1	2	1	3	2	5	3	8	5	13
r3	1		2		3		5		8	
r31	0x100C									

Results of the st instruction.

Memory Address	Contents
8	2
12	3
16	5
20	8
24	13

9. (15 points) Encode the selected statements from the SRC program shown below in hexadecimal. dc means declare character (it makes space for a one byte variable).

```

cnt:    .equ 8
        .org 0
seq:    .dc 1
next:   .dc 1
ans:    .dw cnt
        .org 0x1000
        lar  r31, loop
        la   r0, cnt
        la   r1, seq
loop:   ld   r2, 0(r1)
        ld   r3, 4(r1)
        add  r2, r2, r3
        st   r2, 8(r1)
        addi r1, r1, 4
        addi r0, r0, -1
        brnz r31, r0

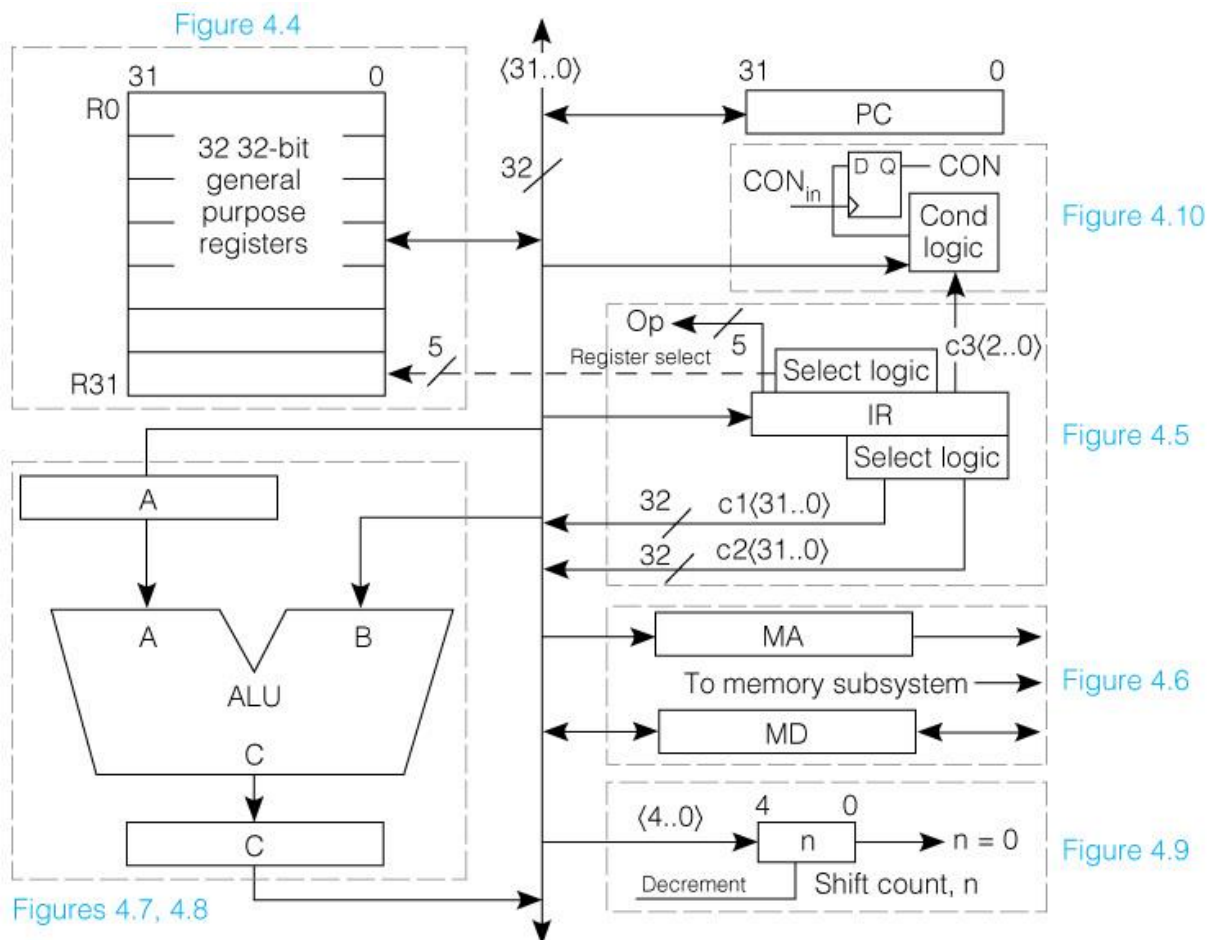
```

Address	Label	Instruction	op	ra	rb	rc	c1	c2	c3	Hexadecimal
0x1004		la r0, cnt	5	0	0	-	-	8	-	0x2800 0008
0x1018		st r2, ans(r1)	3	2	1	-	-	8	-	0x1882 0008
0x101C		addi r1, r1, 4	13	1	1	-	-	4	-	0x6842 0004

10. (25 points) Write the code to implement the expression $A = (((B * C) + D) * E) / F$ on 3-, 2-, 1-, and 0-address machines. Do not rearrange the expression. In accordance with programming language practice, computing the expression should not change the values of its operands.

3-Address	2-Address	1-Address	0-Address
mul A, B, C	load A, B	load B	push B
add A, A, D	mul A, C	mul C	push C
mul A, A, E	add A, D	add D	mul
div A, A, F	mul A, E	mul E	push D
	div A, F	div F	add
		store A	push E
			mul
			push F
			div
			pop A

11. (20 points) Write concrete RTN steps for the SRC instruction `ldr` using the 1-bus SRC microarchitecture shown.



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T0	$MA \leftarrow PC; C \leftarrow PC + 4$
T1	$MD \leftarrow M[MA]; PC \leftarrow C$
T2	$IR \leftarrow MD$
T3	$A \leftarrow C$
T4	$C \leftarrow A + 10@IR\langle 21 \rangle \#IR\langle 21..0 \rangle$
T5	$MA \leftarrow C$
T6	$MD \leftarrow M[MA]$
T7	$R[ra] \leftarrow MD$