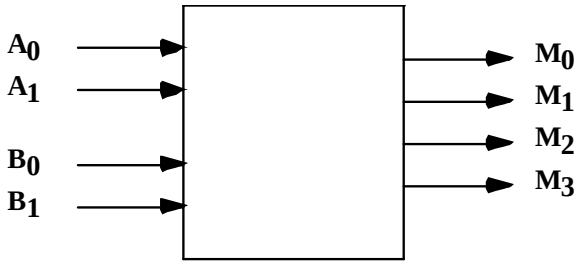
The University of Alabama in Huntsville
Electrical and Computer Engineering
CPE/EE 422/522
Spring 2005
Homework #7
Due 4/21/05

From the book,
10.1 (20 points) (a) & (b) for q s-a-0 and d s-a-1, 10.2 (20 points), 10.7 (10 points)

From other sources
(25 points) Design a hardware multiplier circuit(M) that computes the product of two, positive 2-bit binary numbers.



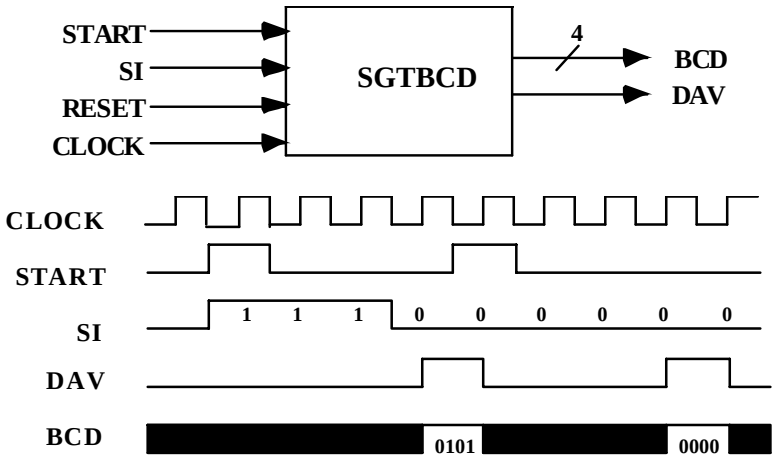
A_1A_0 represents one 2-bit number, B_1B_0 represents the second 2-bit number and $M_3M_2M_1M_0$ represents the 4-bit product. For example, if $A_1A_0 = 10$ and $B_2B_1B_0 = 11$, then $M_3M_2M_1M_0$ –0110. Model your circuit by performing the following steps.

a. Develop a VHDL entity declaration for the multiplier.
b. Develop an algorithmic behavioral architectural body for the multiplier.
c. Simulate to verify the correctness of your model.

(25 points) Design a sequential circuit that converts a 4-bit Gray code into a 4-bit BCD code. The inputs and outputs are timed by the same system clock. Assume that the device receives a START pulse coincident with the left most bit of the Gray code. The remaining bits of the Gray code are received one bit at a time (from left to right). At the end of each 4-bit Gray code, the device outputs the corresponding 4-bit BCD code in parallel along with a DAV signal. The next input could start during the clock period following the last input bit or at any time after that. The device must have a RESET input that initializes the device to the correct starting state. The figure given shows a block diagram and sample timing diagram. Use the table below for the Gray and BCD codes.

Decimal Digit	Gray Code	BCD Code
0	0000	0000
1	0001	0001
2	0011	0010
3	0010	0011
4	0110	0100
5	1110	0101
6	1010	0110
7	1011	0111
8	1001	1000
9	1000	1001

Model the device and do a simulation to verify your model.


START
SI
RESET
CLOCK
SGTBCD
4
BCD
DAV
CLOCK
START
SI
1 1 1 0 0 0 0 0 0
DAV
BCD
0101
0000