The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Fall 2010
Sample Test 2 Solution

1. (1 point) A _prime imiplicant_ is a product term obtained by combining the maximum possible number of adjacent squares in the map.

2. (1 point) Unspecified minterms of a function are called _don't care_ conditions.

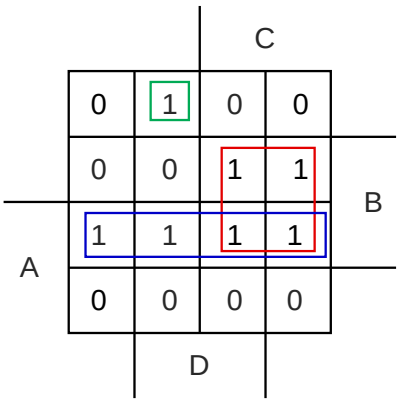
3. (1 point) The _NOR_ operation is the dual of the NAND operation.

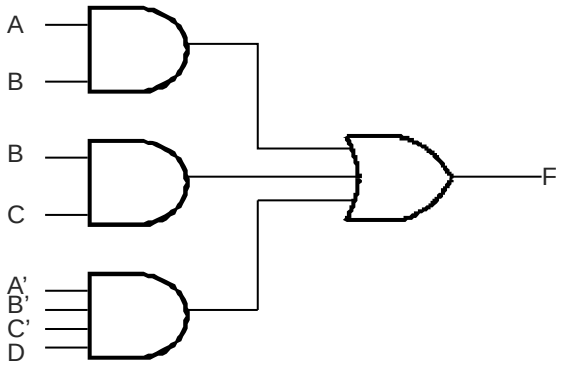
4. (1 point) A _full adder_ is a combinational circuit that forms the arithmetic sum of three bits.

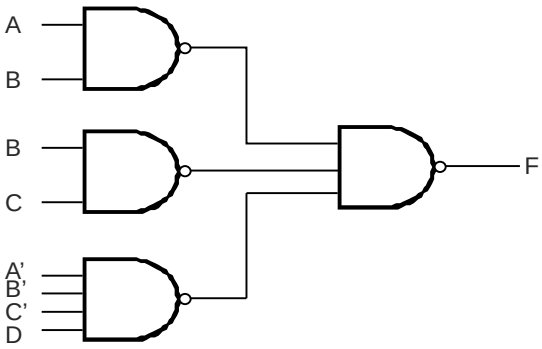
5. (1 point) A _multiplexer_ is a combinational circuit that selects binary information form one of many input lines and directs it to a single output line.

6. (15 points) Simplify the following function and implement it with two-level NAND gates:
   F(A, B, C, D) = AB + A'BC + A'B'C'D

   F(A, B, C, D) = AB + BC + A'B'C'D

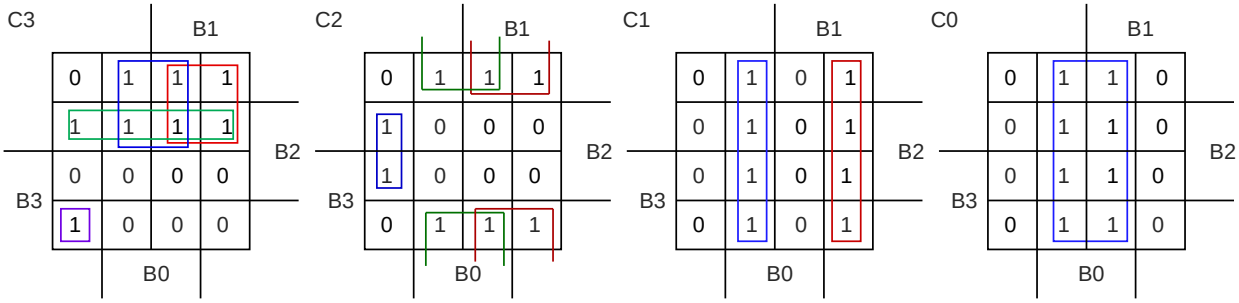






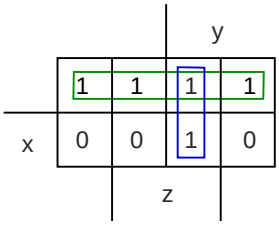
7. (20 points) Design a four-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. You do not need to draw the circuit diagram.

B3	B2	B1	B0	C3	C2	C1	C0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1



C0 = B0
C1 = B1B0' + B1'B0 = B1 ⊕ B0
C2 = B2B1'B0' + B2'B1 + B2'B0 = B2(B1 + B0)' + B2'(B1 + B0) = B2 ⊕ (B1 + B0)
C3 = B3'B2 + B3'B1 + B3'B0 + B3B2'B1'B0' = B3'(B2 + B1 + B0) + B3(B2 + B1 + B0)'
= B3 ⊕ (B2 + B1 + B0)

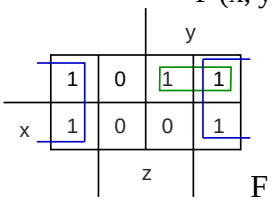
8. (10 points) Simplify the following Boolean expression, using three variable maps:
F(x, y, z) = x'y' + yz + x'yz'



F = x' + yz

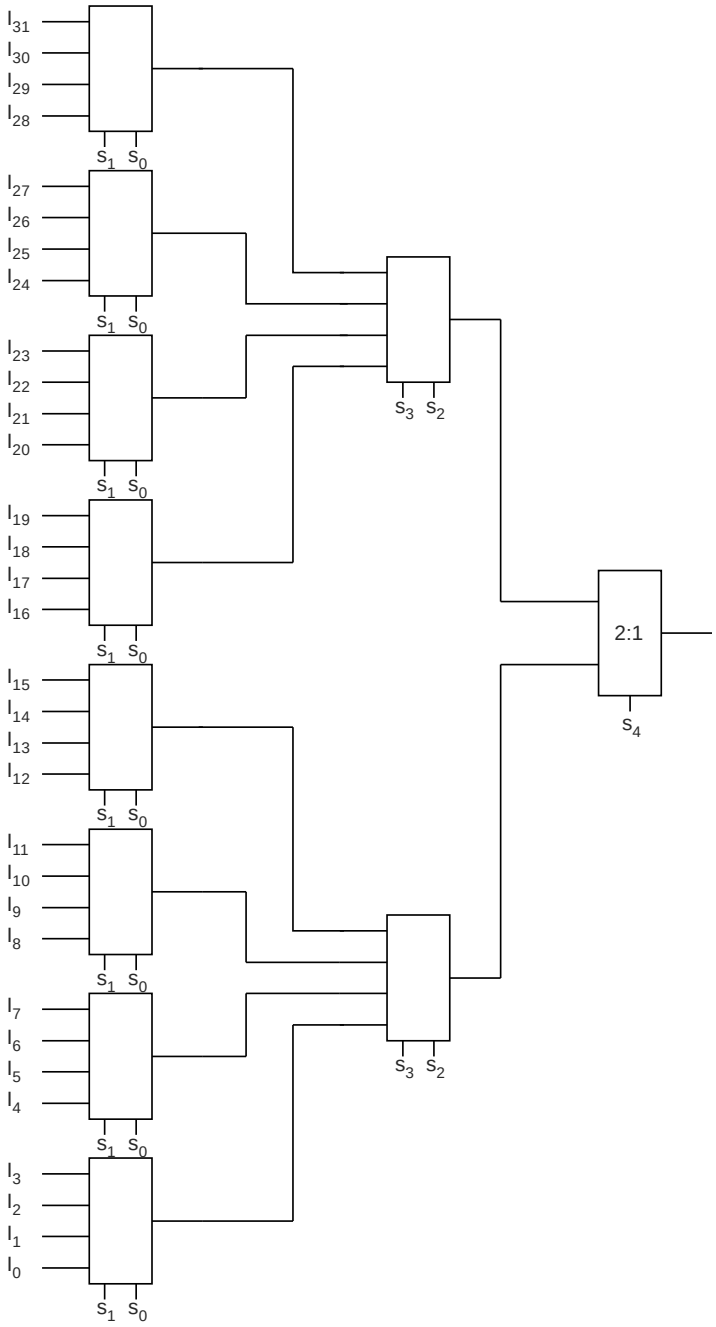
9. (10 points) Simplify the following Boolean function, using three-variable maps:

F (x, y, z) = Σ(0, 2, 3, 4, 6)

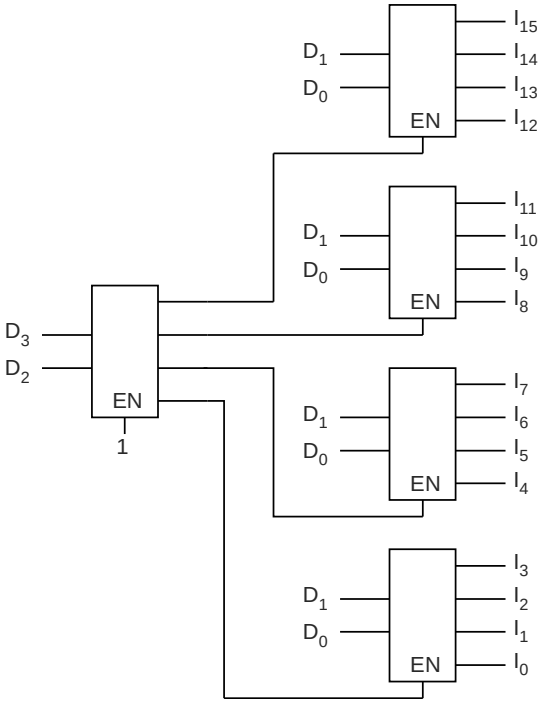


F = z’ + x’y

10. (15 points) Construct a 32 × 1 multiplexer with as many 4 × 1 multiplexers and any additional logic that you might need. Use block diagrams for the components.



11. (10 points) Construct a 4-to-16 line decoder with as many 2-to-4 line decoders with enable as you need. Use block diagrams for the components.



12. (15 points) If the delays in the circuit below are as given in the table, fine the propagation delays from the inputs to C_1 and S_0.

Logic Element	Propagation Delay
Inverter	30 ps
AND/NAND	50 ps
OR/NOR	60 ps
XOR	80 ps

Propagation delay to C_1 = 160 ps, Propagation delay to S_0 = 190 ps